A Study of Multiple-Valued Magnetoresistive RAM (MRAM) Using Binary MTJ Devices

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Abstract

This paper presents four-valued magnetoresistive RAM (MRAM) storage cells using one access transistor and two binary magnetic tunnel junction (MTJ) devices with the MTJ devices either in series or in parallel. We present a comparative study of the two cells in terms of their area and power benefits over the binary MRAM, all using the same conventional MRAM process.

1. Introduction

The widespread adoption of portable computing and communication devices has accelerated the demand for high-density and low-power nonvolatile memory. One of the technologies vying to fill this need is magnetoresistive random access memory (MRAM) based on magnetic tunnel junction (MTJ) devices [1].

The one-transistor-one-MJT-device (1T-1MTJ) cell is the conventional MRAM storage cell. To increase the density of MRAM beyond that of the 1T-1MTJ cell, a four-valued MTJ device has been recently proposed [2]. This proposed cell is based on four-level device technology which is not yet viable. In this paper, we study two implementations of a four-valued MRAM cell which is solely based on binary MTJ devices.

1.1. Review of MTJ Device Operation

An MTJ is a magnetoresistive device whose resistance can be altered by an applied magnetic field. A binary data '1' or '0' is stored in the MTJ device by respectively altering its resistance to 'high' or 'low'. No static power is required to maintain this resistance (state). Figure 1(a) illustrates a simplified cross-sectional view of a conventional MTJ device. The device consists of a tunneling oxide sandwiched between two magnetic layers known as the fixed layer and the free layer. The direction of the magnetic field in the free layer determines whether the device is in the high resistivity state or in the low resistivity state. The difference in resistance of these two states in recent devices [1] is as high as 50%, also known as the magnetoresistance (MR) ratio. The programmable resistance property of the MTJ device is captured in schematics by the symbol in Figure 1(b).

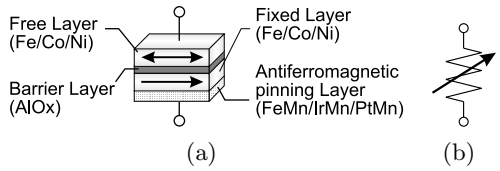

Figure 1. MTJ device (a) cross-sectional view, (b) symbol.

Figure 2(a) shows the schematic of a conventional 1T-1MTJ binary MRAM cell. The cell is read by activating the wordline (WL) and clamping the bitline (BL) to a fixed voltage. Figure 2(b) indicates that a stored logic '1' (high resistivity state) sinks a small current I_R whereas a stored logic '0'(low resistivity state) sinks a large I_R current. A current sense amplifier determines the stored state by comparing the bitline current against a reference current. Typical read currents

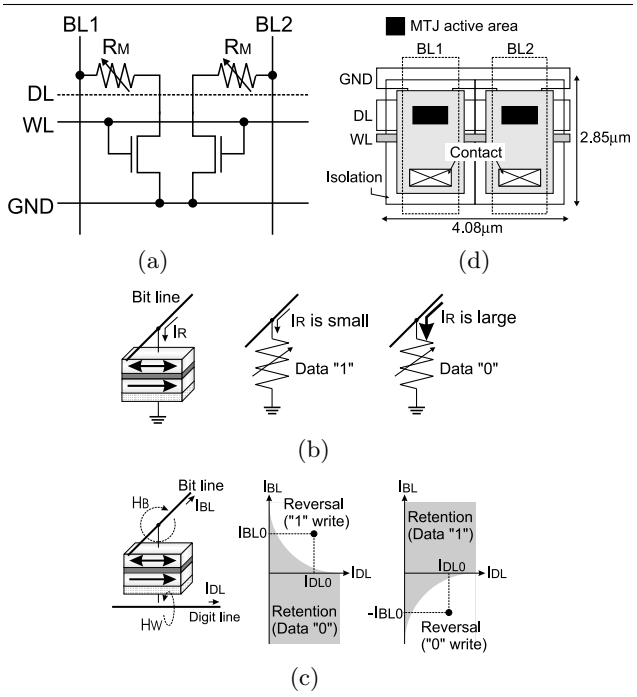

Figure 2. Binary MRAM core cell (a) schematic, (b) read operation, (c) write operation, and (d) layout in a 0.18 µm CMOS technology with an area of 11.62 µm^2

that flow through the MTJ device are not sufficient to change the resistivity state, thus the read operation is nondestructive.

Write operation occurs by forcing a unidirectional current through the digit line (DL) and forcing current through the bitline in one of two directions as shown in Figure 2(c). The intersecting bitline and digit line currents create an overall magnetic field that forces the MTJ device into the high or low resistivity state. A deselected wordline electrically isolates the MTJ device during write operation, ensuring that no current flows through the device.

Figure 2(d) illustrates a sample layout of a binary MRAM cell based on the layout in [3]. This layout is used as the basis for comparison with the multiple-valued MRAM devices presented in this paper.

2. Four-Valued MRAM

We propose and evaluate two implementations of a four-valued core cell that are based on binary MTJ devices. Each cell consists of one access transistor and two binary MTJ devices (1T-2MTJ).

2.1. Core Cell With Series MTJ Devices

Figure 3(a) depicts the schematic of a core cell consisting of one transistor with two MTJ devices in series (series cell). One of the MTJ devices (MTJ2) is twice the area of the other one (MTJ1) and thus MTJ2 has half the nominal resistance of the MTJ1. This configuration results in four possible magnetization states allowing the storage of a two-bit symbol per cell. The MTJ devices are placed on each side of the access transistor to minimize the layout area as shown in Figure 3(b). To read the cell, the control circuitry activates the current path through the two bitlines and the core cell; this current path is depicted in Figure 3(c). A sense amplifier reads the cell by clamping one bitline, grounding the other bitline, and sensing the resulting current. This operation is discussed in more detail in Section 3. Figure 3(d) displays the currents during a write operation. The wordline is deselected and a fixed current is forced on the digit line. The bitline current polarities are set to one of four possible configurations to determine the value written to the cell.

2.2. Core Cell With Parallel MTJ Devices

Figure 4(a) illustrates the schematic of a core cell consisting of one access transistor and two parallel MTJ devices (parallel cell). One of the MTJ devices (MTJ2) is twice the area of the other one (MTJ1) leading to four possible magnetization states for the cell. Figure 4(b) displays the cell layout which requires only a single contact between the MTJ devices and the transistor drain. Eliminating a contact from the layout accounts for the area reduction over the conventional binary MTJ cell. Although the cell is not rectangular, it can be tiled to make full use of the empty area in the bottom right hand corner. Figure 4(c) shows the current path during the read operation in the parallel cell with the access transistor activated. The bitlines are shorted to create a current path from the sense amplifier to ground, through the parallel MTJ devices and the access transistor. For the write operation, the access transistor is deactivated and the appropriate currents are forced through the digit line and the two bitlines as shown in Figure 4(d).

Typically, there is no current traversing through the MTJ device during the write operation. The cell is only affected by magnetic fields. In the proposed parallel device, there can be a small current through the MTJ devices during write if two bitlines have currents that are in opposite directions. Figure 5 illustrates this by using an equivalent circuit. The bitlines are assumed to have a per-cell wiring resistance R_w. When the bitline cur-

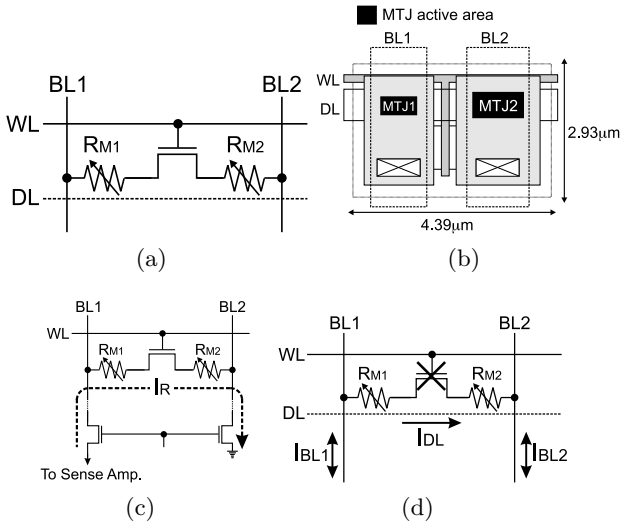

Figure 3. Four-valued MRAM series cell (a) schematic, (b) layout, (c) read operation, and (d) write operation. The core cell area is 12.86 μm^2.

rents, I_{BL1} and I_{BL2}, have different polarity, a small voltage, ΔV, appears across the MTJ devices causing a current, I_{MTJ}, to pass through them. This current can be minimized by limiting the number of cells (m) per bitline such that the maximum ΔV remains below a threshold. Alternatively, writing the MTJ devices independently eliminates this current. We discuss the magnitude of this current further in Section 4.

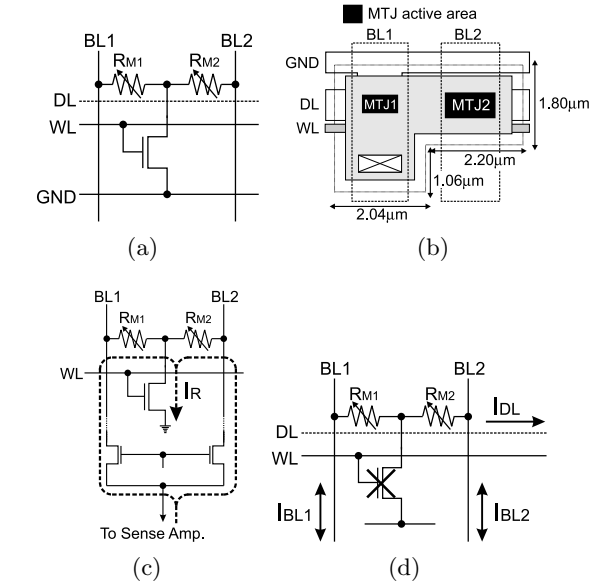

Figure 4. Four-valued MRAM parallel cell (a) schematic, (b) layout, (c) read operation, and (d) write operation. The effective core cell area is 9.79 μm^2.

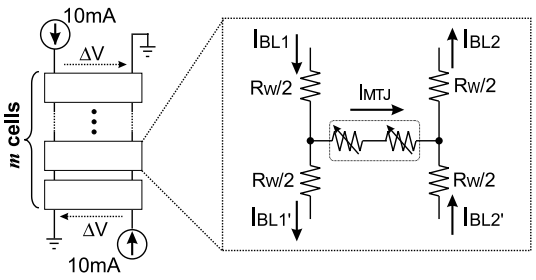

Figure 5. MTJ current during read in parallel cell.

3. Simulation Methodology

The two multiple-valued cells are simulated and compared to the conventional binary 1T-1MTJ cell. Figure 6 shows the common baseline memory architecture [4] selected to establish uniform conditions for simulations of the read access time and the power consumption for all three cases. The memory consists of l blocks, each with m rows and n columns of r-valued cells (where r is either 2 or 4). A column multiplexer, implementing current conveyors, shares a sense amplifier among the n columns in a block. Each block has a reference column that feeds the sense amplifier for reads. In layout, the reference cells would be placed in the centre of a block to minimize the effect of process variation.

Figures 7(a)–(c) show the column and reference circuitry for the binary cell, the series cell, and the parallel cell, respectively. In the reference columns, the MTJ devices are sized and arranged to generate a reference resistance halfway between the resistances of a

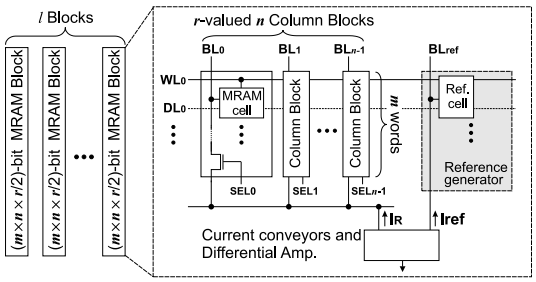

Figure 6. Baseline architecture for comparison of MRAM cells.

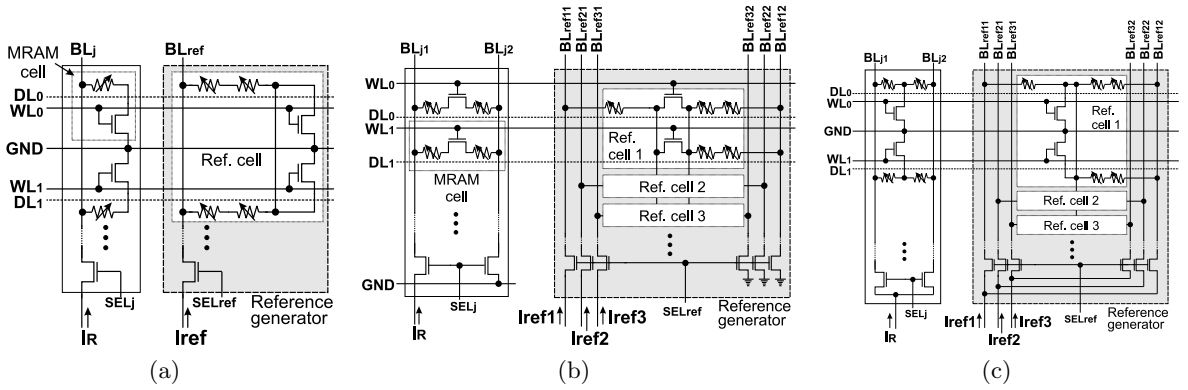

Figure 7. Column circuitry for (a) binary MRAM, (b) multiple-valued MRAM with series cell, and (c) multiple-valued MRAM with parallel cell.

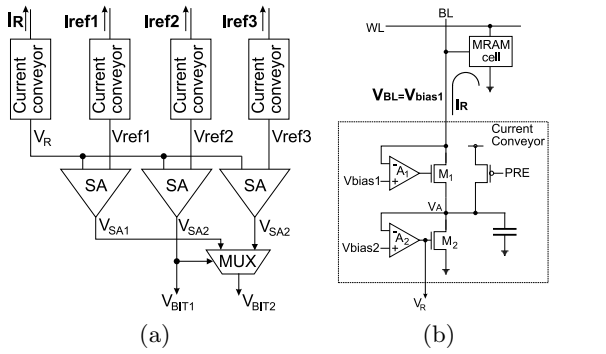

Figure 8. The block diagram (a) of the current conveyors and three sense amplifiers used for the multiple-valued MRAM and (b) the current conveyor.

cell. The reference columns enable the generation of reference currents used by the sense amplifier.

Figure 8(a) shows in more detail the circuits that convert the bitline current to a two-bit logic output. The circuit operates in two stages: first the current conveyors convert bitline currents to voltage signals and then the voltage signals are converted to logic outputs. Figure 8(b) illustrates the schematic of the current conveyors [5]. The current conveyors operate by first clamping the bitline voltage to a fixed voltage V_{bias1} of about 0.6 V. The current conveyors transform the current through the MTJ devices to an output voltage, V_R, which is then compared to the three reference voltages, V_{ref1}, V_{ref2}, and V_{ref3}. These reference voltages are generated from the MTJ devices in the reference cells. Initially, the V_A node is precharged high forcing the V_R node low. The current conveyor operates by using a differential amplifier, A_1, in negative feedback mode to clamp the bitline to V_{bias1}. A current I_R is sunk into the MRAM cell that is proportional to the effective cell resistance. This current causes V_A to fall below V_{bias2}, in turn flipping the polarity of the output of the differential amplifier A_2. Thus V_R rises and turns on the NMOS transistor M_2. The amount of time it takes for V_R to rise depends on the cell resistance. The relative timing of the V_R signal for the active column with respect to the reference columns determines the value of the stored symbol. The V_R, V_{ref1}, V_{ref2}, V_{ref3}, signals feed into the sense amplifiers to generate two-bit logic outputs V_{BIT1} and V_{BIT2}.

In addition to establishing a baseline architecture, we keep the clamped bitline voltage, V_{bias1}, constant across the implementations. Although it is generally preferred to compare RAM implementations by maintaining a fixed sense margin, in this case maximizing the MR ratio is more important because the MR ratio of MTJ devices tends to degrade with applied voltage [3]. We determine that 0.6 V is the largest practical voltage on the bitline and use this value across all implementations in this study.

Figure 9(a) plots the waveforms for a read operation with the series cell. This figure shows the V_A nodes (from Figure 8(b)) and the corresponding V_R, V_{ref1}, V_{ref2}, V_{ref3} outputs of the current conveyors. With V_R being larger than V_{ref1} and V_{ref2}, and smaller than V_{ref3}, V_{SA1} and V_{SA2} fall to ground while V_{SA3} remains at V_{DD}. This is confirmed by the simulation results in Figure 9(b).

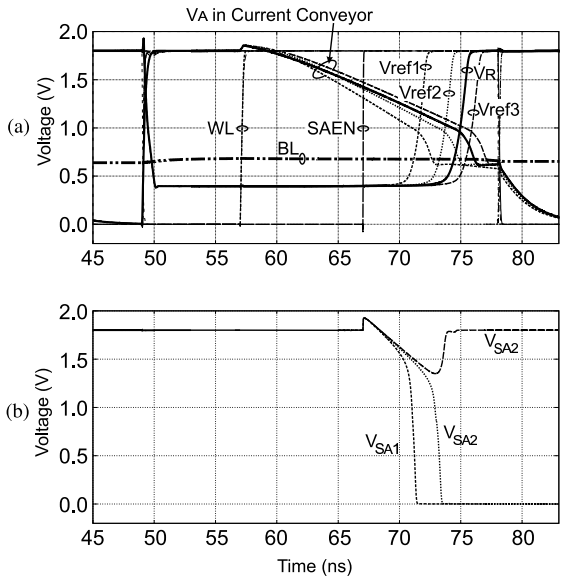

Figure 9. Simulation waveforms for a read in the series cell with (a) current conveyor signals and (b) sense amplifier outputs.

4. Comparative Study

Simulations were performed assuming a conventional 0.18 µm, 1.8 V CMOS transistor technology augmented with MTJ devices. We assume the minimum-sized MTJ device has a high resistance of 90 kΩ and low resistance of 60 kΩ for an MR ratio of 50%. Thus the MTJ devices with twice the area in the multiple-valued cells of Figures 3(b) and 4(b) have a high resistance of 45 kΩ and a low resistance of 30 kΩ. Table 1 summarizes the effective resistances of the three cells under study. Using these values, we revisit the issue of current through the MTJ device during write operation for the parallel cell. Simulation results show that this MTJ current ranges from about 1 µA for 1024 cells per column to 50 nA for 64 cells per column. Depending on the MTJ device tolerance for this current, an optimum number of cells per column can be determined.

	Stored Value			
	'00'	'01'	'10'	'11'
Binary Cell (kΩ)	-	90	60	-
Series Cell (kΩ)	90	105	120	135
Parallel Cell (kΩ)	20	22.5	25.7	30

Table 1. Effective cell resistance for the binary cell, series cell, and parallel cell.

Cell	Read Delay ns / 2-bits	Core Power µW / 2-bits	Core Area μm^2 / 2-bits
Binary	28	497	11.6
Series	29	443	12.4
Parallel	26	472	9.7

Table 2. Simulation results for read operation in binary MRAM, series cell MRAM, and parallel cell MRAM.

Table 2 lists the simulation results for the binary MRAM cell and the two multiple-valued MRAM cells. For a fair comparison, the table lists read delay, core power, and core area normalized to two bits. In terms of read delay and core power dissipation, the three cells are comparable within 12%. The series cell shows marginal improvement in power, but at the expense of increased core area and marginally increased delay. On the other hand, the parallel cell shows marginal improvement in read delay and core area at the expense of power over the series cell. The parallel cell is marginally better than the binary cell for all three parameters.

5. Conclusion

This paper investigates the benefits of using binary MTJ devices to implement four-valued MRAM while avoiding the use of intrinsically multiple-valued MTJ devices. Our study reveals that the parallel cell holds a marginal advantage over the binary cell in terms of read delay, core power, and core area. The series cell holds a slight power consumption advantage over the parallel cell.

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