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A low-distortion oscillator with fast amplitude stabilization

ERIC VANNERSON† and K. C. SMITH†

An improved technique is proposed for stabilizing the output of a variable-frequency RC sine-wave oscillator. Very low harmonic distortion figures and fast amplitude settling are achieved together by sampling the peaks of the output waveform to produce a d.c. voltage having virtually no ripple content. A simplified analysis of the stabilization loop is included, and the effects of non-ideal sampling on distortion are considered.

1. Introduction

A practical sine-wave oscillator cannot be constructed entirely from linear elements, since some form of non-linearity is required to stabilize the output amplitude. This non-linearity usually contributes in some measure to harmonic distortion in the output waveform. When a lamp or thermistor is used to control the output level, for instance, as in the classical Wien bridge, harmonic distortion is considerable at low frequencies because the lamp or thermistor resistance changes significantly over one cycle of the output. Increasing the thermal time constant reduces the distortion, but increases the amplitude settling time. When more precise control of the output level is required than can be obtained with a lamp or thermistor, some form of a.c.-to-d.c. converter is generally used with a voltage-controlled attenuator to regulate the output amplitude by adjusting a feedback gain within the oscillator (Skehan 1968). Just as is the case for the lamp or thermistor, however, it is found that a compromise must be made between harmonic distortion and the response time of the amplitude stabilization mechanism. The problem in this case is to convert amplitude information instantaneously into a d.c. voltage. This d.c. voltage must have as little superimposed ripple as possible, since this ripple, when multiplied by a sinusoid at the fundamental frequency in the voltage-controlled attenuator, will introduce harmonic components into the oscillator output. A low-pass filter can be used following the rectifier, but this results in slower amplitude transient response. If the a.c.-to-d.c. converter is a simple half-wave rectifier, for instance, 0·1% distortion corresponds to an amplitude settling time of several hundred cycles. In an earlier paper (Vannerson and Smith 1974) a method was proposed for reducing the product of settling time and total harmonic distortion by a factor of about 30 by using an improved rectifier having less ripple in its output. Although this is certainly a considerable improvement, a still better method of amplitude regulation is required if quick settling is to be had in combination with distortion limited only by the capabilities of the operational amplifiers used, rather than by the amplitude stabilization system.

One fairly straightforward solution is to replace the rectifier by a sample/hold which samples the oscillator output over some interval around its peak

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† Department of Electrical Engineering, University of Toronto, Toronto, Canada.

(Meyer-Ebrecht 1972). The amplitude regulation system is then a hybrid of discrete-time and continuous-time elements which can be optimized by z-transform methods. The effects of non-ideal behaviour in the sample/hold (such as finite sampling time and decay between samples) on harmonic distortion can be determined by Fourier analysis.

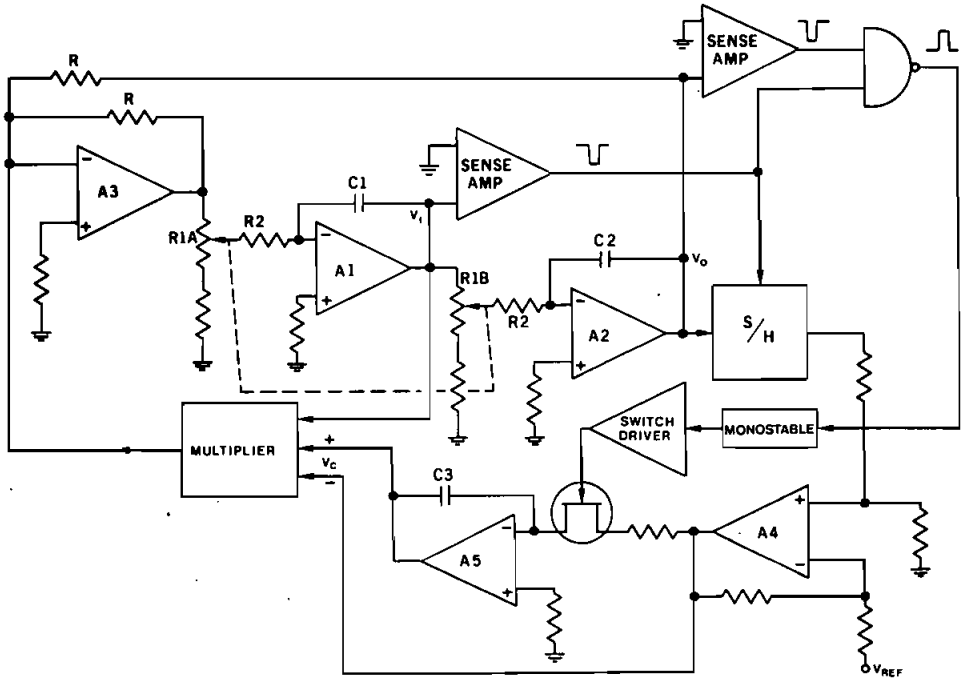

Figure 1. Simplified schematic diagram of the oscillator with amplitude stabilization.

Figure 1 is a simplified schematic diagram showing this method of amplitude regulation. Figure 2 is block diagram of the stabilization system. The oscillator itself is a cascade of two integrators A1 and A2 with an inverter A3. This arrangement can be looked upon as a state-variable filter (Thomas 1971) in which the Q-controlling resistor has been replaced by a current-output analogue multiplier. Dual potentiometer R1 varies the frequency of oscillation

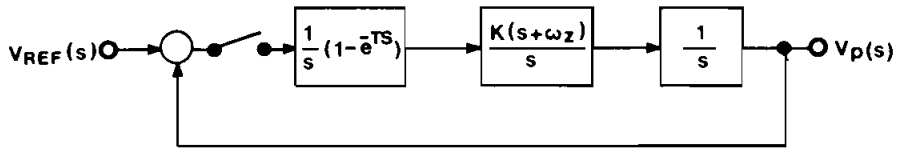

Figure 2. Block diagram of the amplitude stabilization system.

over slightly more than a decade. The output voltage V_0 is sampled at the positive-going zero crossings of V_1, which are coincident with the positive peaks of V_0. The output of amplifier A4 is proportional to the difference between the sampled peak V_p and a reference voltage V_{REF}. This error signal is applied to the multiplier along with its integral from A5.

For optimum performance over a decade of frequency, the integrator gain must be changed in proportion to the oscillator frequency. This can be done conveniently by switching the input resistor into the circuit four times per oscillator period, with a variable duty cycle. The switching waveform is obtained from a monostable multivibrator which is triggered at the zero crossings of the quadrature outputs of the oscillator. Since the switch 'on' time is fixed, duty cycle is proportional to frequency. If the maximum duty cycle is limited to about 50%, the effect is almost that of an integrator input resistor which is inversely proportional to frequency, as required. An exact analysis of the switched integrator is quite tedious. The interested reader should consult Jury (1958), Tou (1959), or Liou (1972).

Duty-cycle control of the integrator is particularly convenient, since pulses at the zero crossings of one output waveform are required to control the sample/hold. The zero crossings of both outputs can be obtained with very little additional hardware.

A simpler and less elegant way to control the integrator gain would be of course to add a third section to the frequency-controlling potentiometer. Since this potentiometer must be of fairly high quality, this alternative is probably not more economical.

2. Analysis of the stabilization loop

An exact analysis of the amplitude stabilization loop can be avoided if only small deviations in output voltage from its steady-state peak value V_{po} are to be considered. It can be shown (Vannerson and Smith 1974) that for small disturbances the response of peak output V_p to a control voltage applied to the multiplier is that of an integrator with transfer function

$$\frac{V_p(s)}{V_c(s)} = \frac{K_m R \omega_0 V_{po}}{2s} \tag{1}$$

where K_m is the multiplier scale factor relating the output current to the input voltages, R is as shown in Fig. 1, and ω_0 is the frequency of oscillation. This result can be derived by approximating exponential changes in output by linear functions.

The sample/hold is equivalent to a sampling switch followed by a zero-order hold, whose transfer function is $[1-\exp(-sT)]/s$, where T is the sampling interval. Note that T can be assumed fixed and equal to the oscillator period, since, if the oscillator poles are near the imaginary axis, the multiplier causes them to move almost horizontally in the s-plane. That is, the oscillator frequency remains nearly constant as the amplitude changes. The overall transfer function is then

$$G(s) = \left[\frac{1-\exp(-sT)}{s}\right]\left[\frac{K_a(s+\omega_z)}{s}\right]\left[\frac{V_{po}K_m R\omega_0}{2s}\right] \tag{2}$$

where K_a is a gain constant associated with the error amplifier. In terms of z, the transfer function is

$$G^*(z) = \frac{(2KT + K\omega_z T^2)}{2} \frac{\left[z - \frac{2KT - K\omega_z T^2}{2KT + K\omega_z T^2}\right]}{(z-1)^2} \tag{3}$$

where

$$K = \frac{K_a V_{po} K_m R \omega_0}{2} \tag{4}$$

The z-plane root locus is a circle which is centred on the z-plane zero and which passes through the double pole at (1, 0). Fast settling will result if the closed-loop poles are placed at the origin, in which case the root locus must be tangent to the imaginary axis. The zero must be positioned at $z = 0{\cdot}5$, hence

$$\frac{2KT - K\omega_z T^2}{2KT + K\omega_z T^2} = 0{\cdot}5 \tag{5}$$

By conventional root locus techniques it is apparent that the gain required to place the poles at the origin is given by

$$\frac{2KT + K\omega_z T^2}{2} = 2 \tag{6}$$

Solving (5) and (6) for KT and $\omega_z T$ gives

$$KT = \tfrac{3}{2} \tag{7 a}$$

$$\omega_z T = \tfrac{2}{3} \tag{7 b}$$

Combining (4) and (7) yields

$$K_a K_m = \frac{3}{2\pi V_{po} R} \tag{8}$$

The response at the sampling instants to a unit step added to V_{REF} is given by

$$C(z) = \frac{G(z)R(z)}{1 + G(z)} = \frac{2z - 1}{z(z-1)} = 2z^{-1} + z^{-2} + z^{-3} + \ldots \tag{9}$$

This response is illustrated in Fig. 3.

3. Harmonic distortion due to non-ideal sampling

Using the loop parameters given by (7), harmonic distortion due to non-ideal properties of the sample/hold can now be assessed. First consider the effect of sampling the oscillator output over a finite interval. Clearly it is desirable to make this interval as long as possible, to improve sampling accuracy and to reduce the bandwidth requirement of the sample/hold. Long sampling times, however, cause the output of the sample/hold to appear as shown in Fig. 4. The sine-wave tip superimposed on the d.c. hold output is injected into the multiplier and causes harmonic components to appear in the oscillator output.

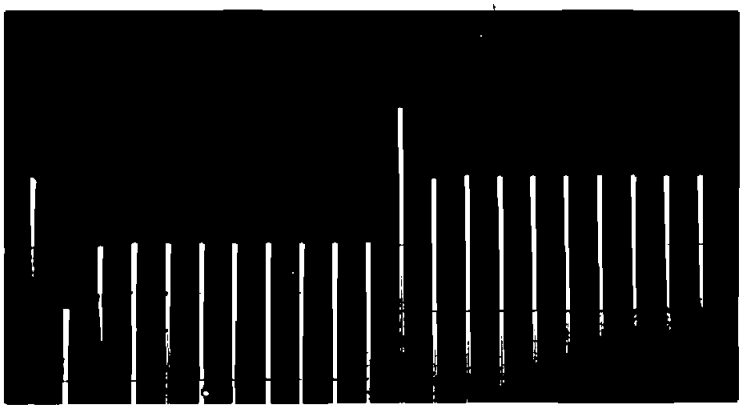

Figure 3. Step response of the stabilization loop.

The sample/hold output of Fig. 4 is given by

$$V_{SH} = \begin{cases} V_p \cos \omega_0 t & [0 < \omega_0 t \leqslant (\pi\tau/T)] \\ V_p \cos (\pi\tau/T) & [(\pi\tau/T) < \omega_0 t \leqslant \pi] \end{cases} \tag{10}$$

where τ is the interval over which the output is sampled. The harmonic-frequency components of the multiplier control voltage are derived almost

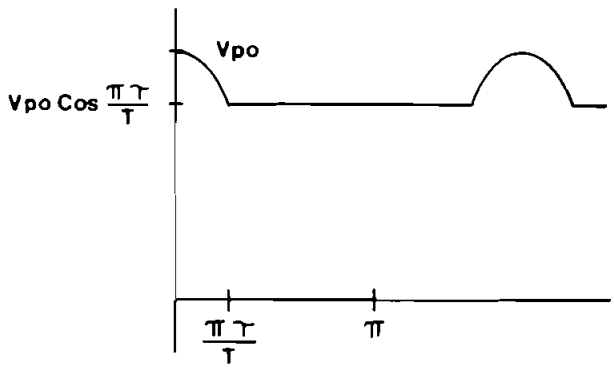

Figure 4. Output of sample/hold for non-zero sampling time.

entirely from the proportional, rather than from the integral, feedback, since, from eqn. (7), ω_z is smaller than ω_0. Therefore the multiplier output current is given approximately by

$$I_0 = \begin{cases} K_a K_m V_p^2 \sin \omega_0 t \cos \omega_0 t & [0 < \omega_0 t \leqslant (\pi\tau/T)] \\ K_a K_m V_p^2 \sin \omega_0 t \cos (\pi\tau/T) & [(\pi\tau/T) < \omega_0 t \leqslant \pi] \end{cases} \tag{11}$$

These functions are odd, hence the Fourier series consists only of sine terms. The coefficients are given by

$$\left.\begin{aligned} b_2 &= \frac{K_a K_m V_{po}^2}{24\pi}(12m\pi - 8\sin 2m\pi + \sin 4m\pi) \\ b_n &= \frac{K_a K_m V_{po}^2}{2\pi}\left[\frac{\sin(n-2)\,m\pi}{(n-2)(n-1)} - \frac{2\sin nm\pi}{(n-1)(n+1)} + \frac{\sin(n+2)\,m\pi}{(n+1)(n+2)}\right] \end{aligned}\right\} \quad (12)$$

where m is the fraction of a cycle over which the output is sampled. The harmonic distortion components are given, in per cent, by

$$D_n = \frac{100 b_n \left|\frac{V_{on}}{I_{on}}\right|}{V_{po}} \quad (13)$$

Combining eqns. (10), (11) and (13),

$$\left.\begin{aligned} D_2 &= \frac{25}{12\pi^2}(12m\pi - 8\sin 2m\pi + \sin 4m\pi) \\ D_n &= \frac{75}{\pi^2(n^2-1)}\left[\frac{\sin(n-2)\,m\pi}{(n-2)(n-1)} - \frac{2\sin nm\pi}{(n-1)(n+1)} + \frac{\sin(n+2)\,m\pi}{(n+1)(n+2)}\right] \end{aligned}\right\} \quad (14)$$

Total harmonic distortion can be computed by summing D_n over n and taking the square root of the result. The result, which is plotted against m in Fig. 5, can be approximated quite well by

$$\mathrm{THD} = 503m^5 \quad (15)$$

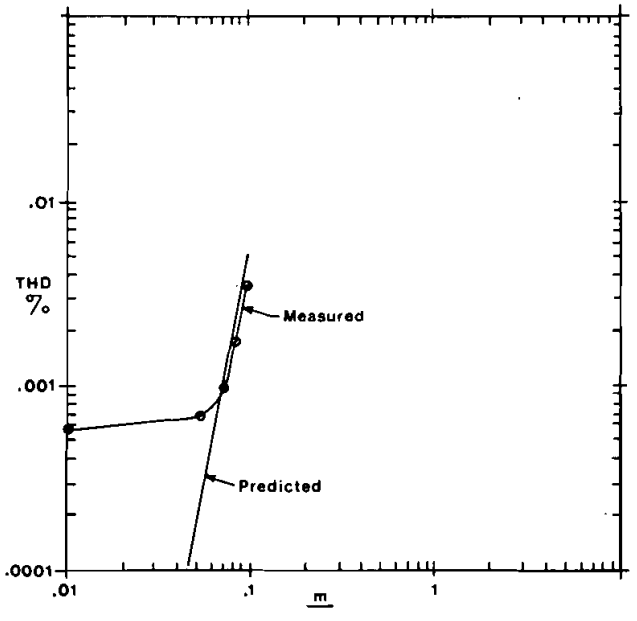

Figure 5. Distortion versus normalized sampling time.

Figure 5 also shows measured distortion, which agrecs reasonably well with eqn. (14) so long as the predicted distortion is substantially greater than the distortion due to other causes, such as amplifier non-linearities. It may be surprising to note that the sampling pulse can be as wide as $0{\cdot}05T$ without increasing the distortion greatly above its minimum value.

Another source of distortion is the decay of the sampled amplitude between samples. This decay can be reduced by increasing the size of the storage capacitor in the sample/hold, but this results in longer settling times in the sample mode. It is therefore desirable to know how much decay is tolerable.

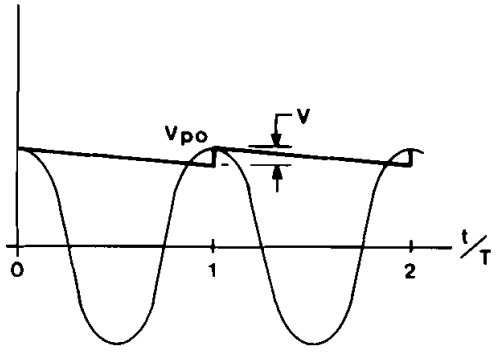

Figure 6. Output of sample/hold showing decay between samples.

The sample/hold output is shown in Fig. 6. If V is small compared to V_{po}, as it must be if distortion is to be small, the output decay is given approximately by

$$V_{SH} = -\frac{V\omega_0 t}{2} \tag{16}$$

The multiplier output current is

$$I_0(t) = \frac{K_a K_m V_{po} V\omega_0 t}{2} \sin \omega_0 t \quad [-\pi < \omega_0 t \leqslant \pi] \tag{17}$$

Using (8),

$$I_0(t) = \frac{3V\omega_0 t}{4\pi^2 R} \sin \omega_0 t \quad [-\pi < \omega_0 \tau \leqslant \pi] \tag{18}$$

This is an even function, and

$$|a_n| = \frac{3Vn}{2\pi^2(n^2-1)} \tag{19}$$

The nth harmonic distortion component, in per cent of the fundamental, is

$$D_n = \frac{100|a_n| \left|\frac{V_{on}}{I_{on}}\right|}{V_{po}} \tag{20}$$

From eqns. (13), (19) and (20),

$$D_n = \frac{150\,Vn}{\pi^2 V_{po}(n^2-1)^2} \tag{21}$$

Summing as before over n gives

$$\text{THD} = 2{\cdot}773 \left| \frac{V}{V_{po}} \right| \tag{22}$$

This expression has been found to agree quite well with experimental results. If this distortion is to be reduced to the level of the measured residual due to other causes (about 0·0005%), leakage from the storage capacitor must be very small. For $V_{po} = 10$, the decay over one cycle must be no more than 1·8 millivolts.

Since the amplitude settling time is limited by the sampling rate, one might reasonably consider sampling more frequently, say twice per cycle. This could be done by sampling V_0 alternately with the output of inverter A3. However, a small amplitude difference or d.c. offset between the two inputs to the sample/hold would be disastrous. The maximum allowable value of the difference between alternate samples is of the same order of magnitude as the amount of allowable sag, that is, not more than a few millivolts for a distortion contribution equal to the residual due to other causes. It would be rather difficult in practice to achieve a d.c. offset this small, and it would be virtually impossible to match the two amplitudes correspondingly well.

4. Conclusion

The oscillator with sample/hold amplitude stabilization has been shown to perform quite well. It is capable of extremely low distortion (limited only by the amplifiers used in the oscillator itself) and fast amplitude settling (two oscillator periods). The principle is applicable not only to general-purpose laboratory oscillators, but especially to automated test systems requiring fast-settling sinusoids. Remote frequency control can be accomplished by replacing the tuning potentiometers by analogue multipliers for analogue control signals or by multiplying DAC's, digitally controlled amplifiers (Sedra and Smith 1969) or digitally controlled potentiometers for digital control.

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