TERNARY LOGIC IN A POSITIONAL CONTROL SYSTEM

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Abstract

The application of COS/MOS integrated circuits in the construction of a three-valued positional control system is presented. A unit-distance ternary code and the design of a ternary encoder are given. A ternary code converter able to translate this unit-distance code to the signed ternary code is described. A ternary threshold level detector is required to convert a noisy, slowly-changing, analog voltage into an abrupt digital logic change at required threshold levels. A three-valued comparator is constructed to compare the reference signal with the one fed back, and to supply an error signal. The logic design of the ternary control circuit is also presented.

1. Introduction

In digital process control the required outputs are basically ternary, e.g., for a digital shaft servo three commands are needed: no error, remain in position; counter-clockwise error, rotate clockwise; and clockwise error, rotate counter-clockwise. For this and other reasons, three-valued logic may be applied in the design of control systems with reduction of circuit complexity. Though this fact has been realized, few attempts have been made in this direction[1-3].

In this paper, the application of COS/MOS integrated circuits in the construction of a three-valued positional control system is presented. A suitable unit-distance code and the logical design for the necessary code conversion is given. The design of a ternary comparator as well as a ternary control circuit are discussed.

2. Ternary Positional Control System

The system is composed of a servo motor with a shaft-mounted encoder which translates angular shaft position into digital signals by means of a photo-electric system. A ternary threshold level detector accepts these signals and supplies them to a code converter which feeds one input of a ternary comparator. The second input of the comparator is a reference signal representing the position required by the system. A ternary control circuit takes the output from the comparator and controls the servo motor. This is represented in Figure 1.

Ternary elements used in this study are based on the operators given in references 4 and 5. Their definitions are listed in the Appendix. The three states -1, 0 and +1, are physically represented by -4, 0 and +4 volt signals, respectively.

3. The Encoder

The ternary encoder proposed here is a simple optical encoder with direct transmission. It is composed principally of a disk having three levels: Opaque, partially opaque and transparent. Reading is realized by means of photo-electric cells coupled to ternary detectors. Each track on the disk has one photo-electric cell which is coupled to one ternary detector. The position of the shaft with reference to the radial line containing the photocells is read by projecting a beam of light at the photocells. This passes through the disk and the outputs of the cells give the position of the motor shaft as a ternary number. Thus, the outputs of the cells provide a contiguous indication of the ternary number representint the shaft position as the shaft rotates.

To eliminate ambiguity in the encoder a unit-distance code must be used. In this code the representation of two consecutive numbers is different in only one position. Furthermore, it is critical (when chosing a suitable unit-distance code) that the output of the transducer cannot pass from state -1 to state +1 without passing through state 0[1], otherwise an ambiguity of detected states is possible. Table I shows the proposed unit-distance ternary code.

4. The Ternary Threshold Level Detector

The function of the threshold level detector is to convert a slowly changing analog voltage into an abrupt digital logic change at the required threshold levels. Since signals taken from the encoder photo-electric cells may be noisy and have slow transition times, a ternary detector is required at the output of each photo-electric cell. The detector is designed to supply an output related to the input signal as shown in Figure 2. The function of the ternary detector may be easily realized by cascading two STI circuits as shown in Figure 3. The output Q is given by:

$$Q = \begin{cases} V_{DD} & \text{if } V_{in} > V_{UT} \\ 0 & \text{if } V_{UT} \geq V_{in} \geq V_{LT} \\ V_{SS} & \text{if } V_{in} < V_{LT} \end{cases}$$

where $V_{DD} > V_{UT} > V_{LT} > V_{SS}$,

V_{DD} is the drain voltage (+4V),

V_{SS} is the source voltage (-4V),

V_{UT} and V_{LT} are the upper and lower threshold values.

This circuit is used also as a buffer between the encoder and code converter.

5. The Code Converter

It is appropriate to convert the encoder output signal to a signed ternary code before passing it through the comparison circuit. For this conversion, the most significant trit x_n will remain as it is and the next most significant trit x_{n-1} will be simply inverted if x_n is 0. Similarly, for x_{n-2} when x_{n-1} is 0, and so on.

A straightforward method to implement this function is to use T-gates as the basic elements in the converter (Figure 4). The T-gate function is defined by

$$T(a_-, a_0, a_+; S) = a_i$$

where i is -, 0 or + when S takes on the values of -1, 0 or +1 respectively. However, we should note that such circuits tend to result in rather complex configurations.

The code converter proposed here is considerably simpler. It has a ternary code converter cell (TCCC) as the essential element. This is composed of one STI circuit and two ternary switches (TS) connected as shown in Figure 5b. The TS, which is shown in

Figure 5a., will be a short circuit if its control voltage V_C is positive (+4 volts) and open circuit if V_C is negative (-4 volts). The circuit diagram of this TS was presented in reference 5. The unit-distance to signed ternary code converter is composed of the TCCC and the $J_0(X)$ operators connected in a triangular array form as shown in Figure 6. The number of TCCC circuits (N) necessary to convert n trits of unit-distance code is given by:

$$N = \sum_{i=1}^{n-1} i$$

Although this number is equal to the number of T-gates necessary to convert the same ternary number using the converter of Figure 4, the construction of the TCCC itself is much simpler than that of the T-gate.

6. Three-valued Comparator

The signal coming from the feedback path and representing the present shaft position has to be compared with a reference signal representing the required shaft position. The comparator compares these two signals and determines which is larger, thus determining the direction of the corrective rotation to cancel the error.

A ternary comparator unit (TCU), able to compare two trits x and y, is given in Figure 7a. It is composed of a T-gate, NTI, STI, PTI, Forward diode and reverse diode connected as shown. The output C is equal to +1 if $x > y$, 0 if $x = y$ and -1 if $x < y$. Performance of the TCU is described by the truth table shown in Figure 7b. It has to be noted that the three types of ternary inverters forming the TCU will be practically substituted by only one COS/MOS ternary inverter[4-5].

To compare two ternary numbers, each composed of n trits, it is necessary to have n TCU's to compare each trit separately and n-1 T-gates to determine which output of the n TCU's will be taken as the error signal. The TCU_n, which compares the two most significant trits, will give the error signal if its output is +1 or -1. If its output is equal to 0 the output of TCU_{n-1} will be taken as the error signal (if it is +1 or -1). Again if the latter is equal to 0 the output of TCU_{n-2} will be taken under the same conditions, and so on. An example of a 4-trit comparator is given in Figure 8. Note that the ternary comparator gives only the direction of the correcting rotation. It can be substituted by a full ternary subtractor to supply varying magnitudes of the error signal. In this case other circuits are required for proper operation, such as stabilizing circuits, which make the system more complex and costly.

To guarantee correct operation of the circuit it is necessary to synchronize input and output signals of the proposed ternary comparator. An additional simple circuit is used. The control pulse (low to high) required for entering the reference signal R to the comparator may be inverted through a delay element which controls a TS inserted in the output of the comparator. The delay element is introduced to the circuit by means of a ternary monostable composed essentially of two crosscoupled TNOR gates (as shown in Figure 9). The delay time of the added element must be greater than the total delay time for a signal to propagate from TCU(4) to TCU(1). The output of the ternary comparator will be blocked only while the reference signal R is entering and for a period equal to the propagation delay time of the added delay element.

7. The Ternary Control Circuit

The error signal taken from the ternary comparator drives the ternary control circuit which gives the necessary control signals to the servo motor. The block diagram of the ternary control circuit is given in Figure 10. It is composed of two NTI circuits, two PTI circuits and one STI circuit driving two pairs of complementary discrete bipolar transistors T_1 - T_4. Taking advantage of the construction of the ternary COS/MOS inverter[5], the five ternary inverters shown in Figure 10 can be replaced by only three. The NTI(1) and PTI(1) can be replaced by only one ternary inverter; the NTI(2) and the PTI(2) by a second one. The schematic diagram of this control circuit may then be reduced to the circuit of Figure 11.

When the error signal E is 0, the P and N channel transistors of Q_1 and Q_2 are on and points A_1 and A_2 are at +4V; B_1 and B_2 at -4V; thus the four transistors T_1 - T_4 will be off and the servo motor will not rotate in either direction. If E becomes +1 the N channel transistor of Q_1 and P channel of Q_2 will be on, making transistors T_1 and T_4 on while T_2 and T_3 will be off. In this case C_1 will be positive with respect to C_2 and the servo motor will have a control signal to rotate clockwise. If E becomes -1 the opposite case will be reached. In this case transistors T_2 and T_3 will be on while T_1 and T_4 will be off making C_1 negative with respect to C_2 and the servo motor will have a control signal to rotate counter-clockwise.

8. Conclusion

The application of COS/MOS integrated circuits in the construction of the three-valued positional control system is shown to be feasible. This system realization is simpler than the corresponding binary one, with apparent economic advantages. However, precision and stability were not included in this study and further research in this direction is recommended.

References

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Appendix

The three-valued operators used in this paper are five unary operators: the simple ternary inverter (STI), the positive ternary inverter (PTI), the negative ternary inverter (NTI), the forward diode (FD), the reverse diode (RD); the two multiple input operators: the ternary NAND (TNAND) and the ternary NOR (TNOR). They are defined as follows:

$$STI \equiv \overline{x^0} = -x$$

$$PTI,\ NTI \equiv \overline{x^i} = \begin{cases} i & \text{if } x \neq i \\ -i & \text{if } x = i \end{cases}$$

where i takes on the value +1 for the PTI and -1 for the NTI operator.

The minus sign in these two equations represents arithmetic negation.

$$FD,\ RD \equiv x^{K_i} = \begin{cases} 0 & \text{if } x \neq i \\ i & \text{if } x = i \end{cases}$$

where i can be +1 or -1, K_{+1} represents the FD operator ($\neg$) and K_{-1} the RD operator ($\sim$).

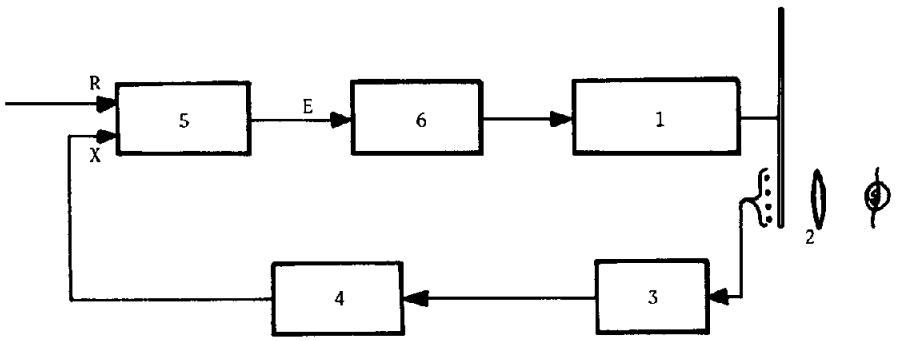
$$TNAND \equiv \overline{(x \cdot y)^0} = \overline{MIN(x,y)^0}$$

$$TNOR \equiv \overline{(x + y)^0} = \overline{MAX(x,y)^0}$$

Circuits for these operators as well as other functional building blocks described in this paper have been presented in reference 5. These circuits were designed with commercially available COS/MOS integrated circuit packages, namely the CD4007 and the CD4016.

Decimal	Signed Ternary Code			Unit-Distance Ternary Code		
	x_3	x_2	x_1	x_3'	x_2'	x_1'
-4	0	-1	-1	0	+1	+1
-3	0	-1	0	0	+1	0
-2	0	-1	+1	0	+1	-1
-1	0	0	-1	0	0	-1
0	0	0	0	0	0	0
+1	0	0	+1	0	0	+1
+2	0	+1	-1	0	-1	+1
+3	0	+1	0	0	-1	0
+4	0	+1	+1	0	-1	-1
+5	+1	-1	-1	+1	-1	-1
+6	+1	-1	0	+1	-1	0
+7	+1	-1	+1	+1	-1	+1
+8	+1	0	-1	+1	0	+1
+9	+1	0	0	+1	0	0
+10	+1	0	+1	+1	0	-1
+11	+1	+1	-1	+1	+1	-1
+12	+1	+1	0	+1	+1	0
+13	+1	+1	+1	+1	+1	+1

Table I: A unit-distance ternary code



1 - servo motor
2 - encoder
3 - threshold level detector
4 - code converter
5 - comparator
6 - control circuit

Figure 1
Ternary positional control system

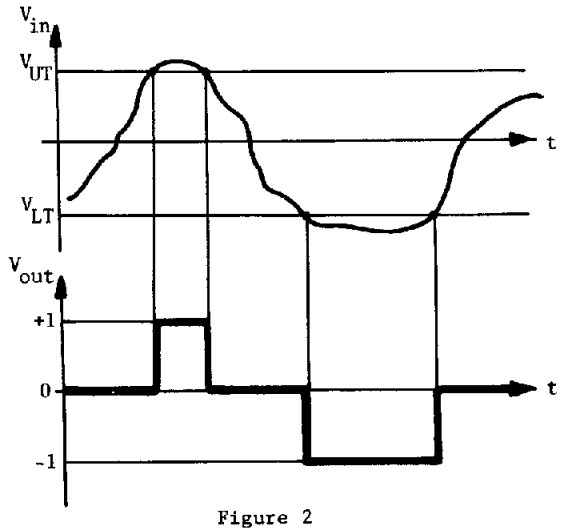


Figure 2
Input-output wave forms of a ternary threshold level detector

Figure 3
Two cascaded STI as ternary threshold level detector

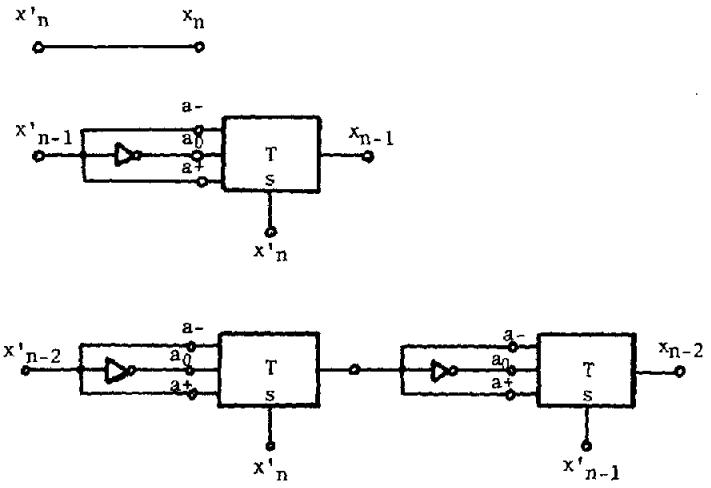


Figure 4
The unit-distance to signed ternary code converter designed with T-gates

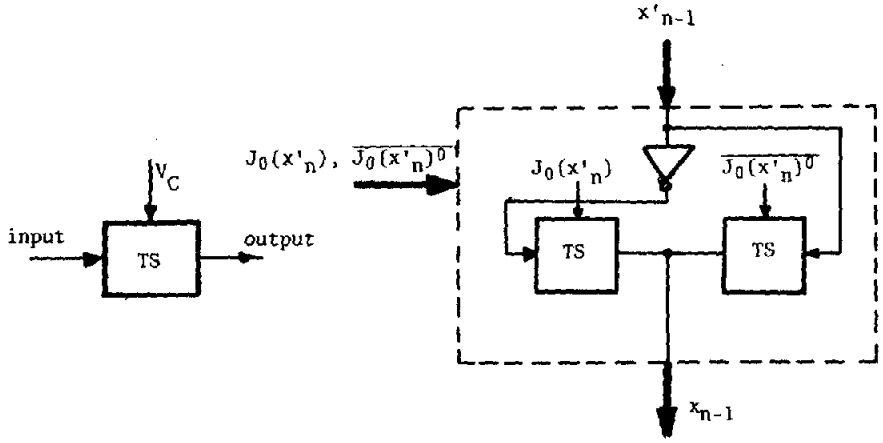


Figure 5
(a) Symbolic diagram of a ternary switch (TS)
(b) Block diagram of a ternary code converter cell (TCCC)

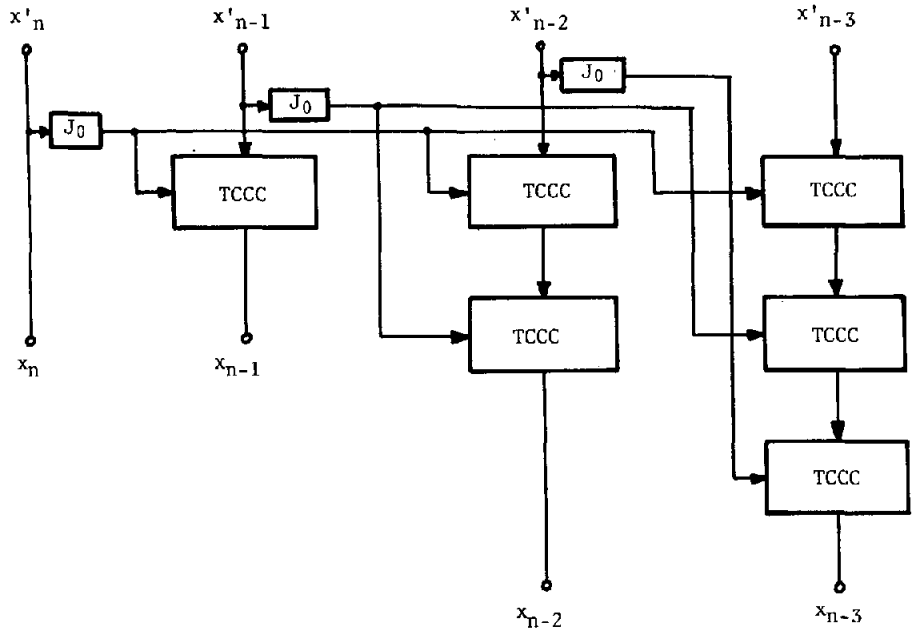
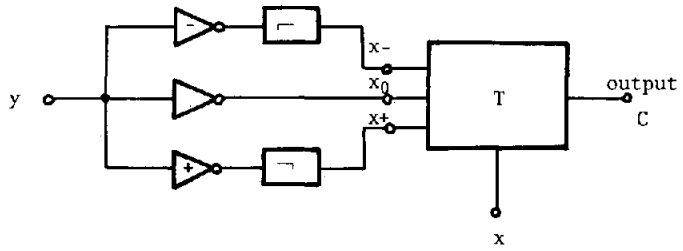


Figure 6
The unit-distance to signed ternary code converter



(a)

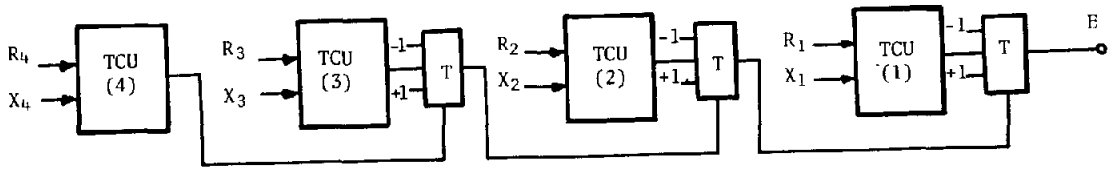
x \ y	+1	0	-1
+1	0	+1	+1
0	-1	0	+1
-1	-1	-1	0

(b)

(a) The ternary comparator unit (TCU)

(b) Truth table for operation of the TCU

Figure 7



A 4-trit ternary comparator

Figure8

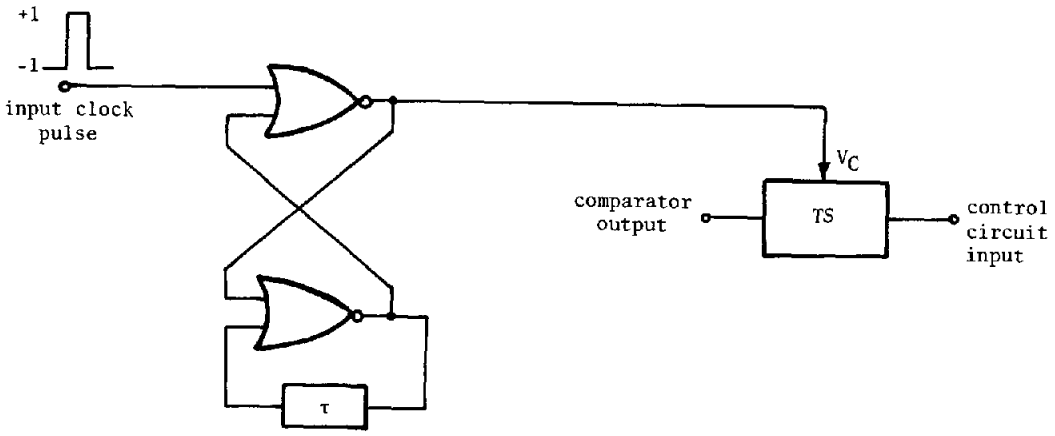


Figure 9
Synchronizing circuit

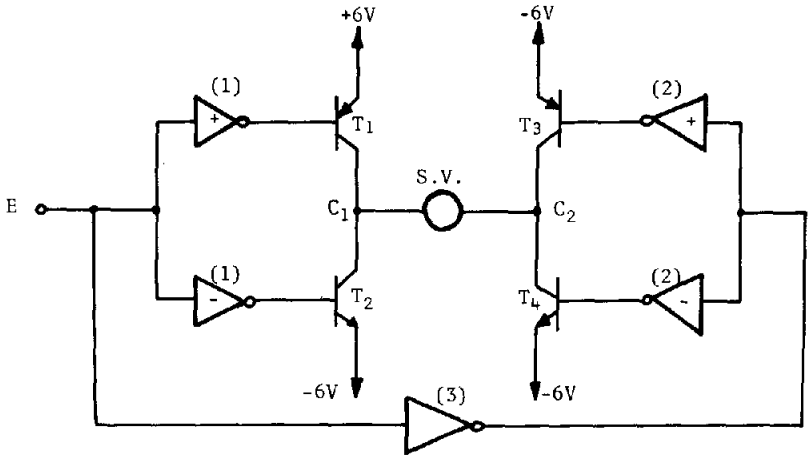


Figure 10
Block diagram of the ternary control circuit

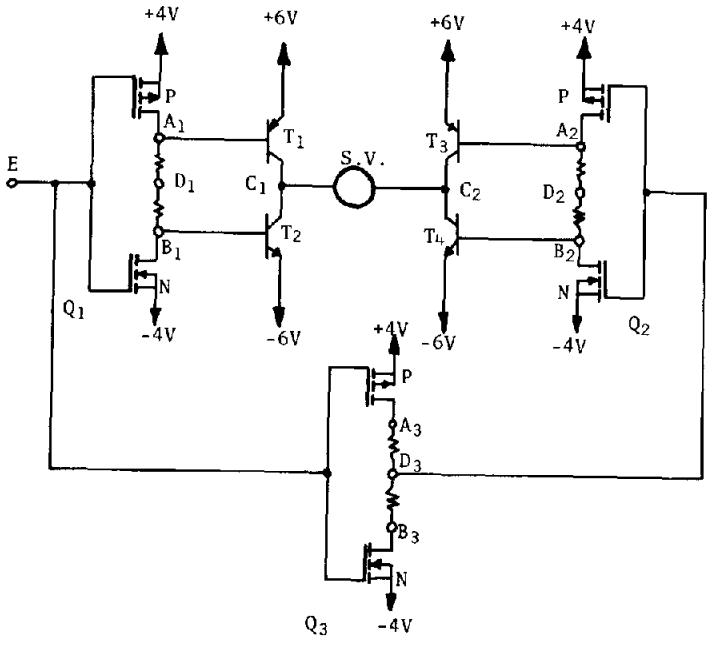


Figure 11
Schematic diagram of the ternary control circuit