Design and implementation of three-valued logic systems with m.o.s. integrated circuits

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Abstract: A method of design of three-valued logic circuits which reduces the need for complementary pairs of m.o.s. integrated circuits is presented. Circuits of basic ternary operators (inverters, NAND and NOR) are utilising single m.o.s. transistors. Based on these ternary operators it is possible to design simpler and cheaper three-valued logic systems. As examples, the construction of the J_k arithmetic circuit and the T-gate are described.

1 Introduction

Recently, the complementary metal-oxide semiconductor family of integrated circuits (c.m.o.s.) has been used by several authors in the realisation of three-valued logic circuits.[1-8] In all previous designs authors have used complementary pairs of p and n channel transistors in some symmetrical fashion to get the three different logic levels. In most cases, this has introduced some redundancy and complexity in the circuits. A systematic method of designing three-valued logic systems using m.o.s. transistors, not necessarily in complementary pairs, is presented. The new design reduces complexity and cost, and shows better performance.

2 Methodology

The ternary inverter of Fig. 1[1,2] has proven to be the simplest ternary functional block that has been proposed. The circuit is composed of one p-channel and one n-channel enhancement-type m.o.s. transistor and two resistors. In one practical version, the source of the p-channel transistor is connected to a $+4$ V power supply and the source of the n-channel is connected to -4 V. The drains of the two channels are connected to each other by means of two equal resistors, R_1 and R_2. The point D shown on the Figure represents the output of the simple ternary inverter (s.t.i.). When only the p-channel device conducts, D is at a high level ($+4$ V). When the n-channel device alone conducts, D is at a low level (-4 V). When both conduct, D is at an intermediate level (0 V). Following one of many possible conventions we shall label the lower, middle and upper levels, logic 0, 1 and 2 respectively. Thus the output at D is defined by

$$\overline{x^1} = 2 - x \tag{1}$$

On the same Figure, point A represents the output of the positive ternary inverter (p.t.i.) and point B the output of the negative one (n.t.i.). These inverters are defined later in the text.

From the Figure it is clear that the circuit is composed of two distinct binary parts. The first part, namely the p-channel transistor, performs the positive logic function of the unit. It provides the positive logic level (level 2) when it is activated. The second binary part of the circuit, namely the n-channel transistor, provides the negative logic level (level 0) when it is activated, performing the negative logic function of the unit.

3 Implementation

Following this reasoning, one can split the circuit of Fig. 1 into two separate circuits as shown in Fig. 2*a* and *b*. The circuit of Fig. 2*a* in fact realises the function of a positive ternary inverter which is defined by

$$\overline{x^2} = \begin{cases} 2 & \text{if } x \neq 2 \\ 0 & \text{if } x = 2 \end{cases} \tag{2}$$

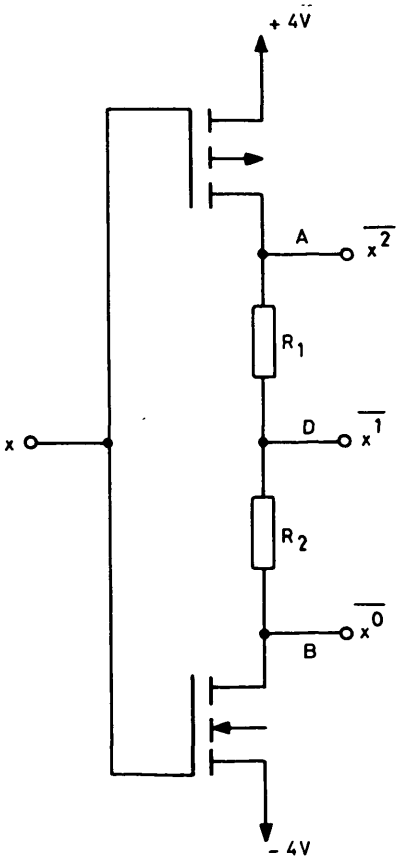

Fig. 1 *C.M.O.S. ternary inverter*
$R_1 = R_2 = 12\ \text{k}\Omega$
A: output of p.t.i.
B: output of n.t.i.
D: output of s.t.i.

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The output of the inverter is taken from the drain of a p-channel transistor that is also connected to the negative power supply through resistor R. The switch (p-channel) is closed if its gate x takes the value 0 or 1, fixing the output at the voltage of its source, + 4 V (level 2). The output goes low (level 0) when the gate is placed at level 2, opening the switch. It is clear that the number of elements realising the p.t.i. circuit of Fig. 2*a* is half of that of Fig. 1, thus indicating a direction for reducing the cost of ternary logic circuit implementations.

Fig. 2*b* shows the realisation of an n.t.i. circuit with a single n-channel transistor and a single resistor. The function of the n.t.i. is defined by

$$\overline{x^0} = \begin{cases} 2 & \text{if } x = 0 \\ 0 & \text{if } x \neq 0 \end{cases} \tag{3}$$

The output goes low (level 0) when the input is at level 1 or 2, that is when the switch (n-channel) is closed. The switch will be open only when its gate takes the value of 0, making the output go high (level 2). Again it is clear that the number of elements realising the n.t.i. circuit of Fig. 2*b* is always half of that of Fig. 1.

A ternary NOR (TNOR) circuit was also presented previously.[1,2] The two-input TNOR circuit is composed of two p-channel m.o.s. transistors connected in series and two n-channel m.o.s. transistors connected in parallel. The two p-channels are connected to the two n-channels by means of two resistors R_1 and R_2 exactly in the same way as the ternary inverter shown in Fig. 1. Similar to the ternary inverter, three outputs are also provided for realising the functions of the simple TNOR, the positive TNOR and the negative TNOR which are defined as

$$\overline{(xVy)^i} = \overline{\{\max(x, y)\}^i} \tag{4}$$

where $i = 1$ for the simple TNOR, 2 for the positive TNOR, and 0 for the negative TNOR.

By following the same technique adopted above, the TNOR circuit could also be split into two separate circuits, one for the positive TNOR (Fig. 3*a*) and one for the negative TNOR (Fig. 3*b*). The positive TNOR is composed of two p-channels and a resistor connected in series as shown in Fig. 3*a*. The output Z produces the positive inversion of the maximum value of the two inputs. The negative TNOR is composed of two parallel n-channels connected to a resistor as shown in Fig. 3*b*. In this case the output produces the negative inversion of the maximum value of the two inputs.

The same idea is applied also to the ternary NAND (TNAND) circuit[1,2] which is a complement of the TNOR circuit in its construction. The simple TNAND, the positive TNAND and the negative TNAND which result are defined as

$$\overline{(x\Lambda y)^i} = \overline{\{\min(x, y)\}^i} \tag{5}$$

where $i = 1$ for the simple TNAND, 2 for the positive TNAND, and 0 for the negative TNAND.

As above, by dividing the TNAND circuit into two separate circuits, the two circuits of Fig. 4*a* and *b* can be obtained. The output of the positive TNAND (Fig. 4*a*) produces the positive inversion of the minimum value of the two inputs. The output of the negative TNAND (Fig. 4*b*) produces the negative inversion of the minimum value of the two inputs.

It is obvious that the above TNOR and TNAND circuits

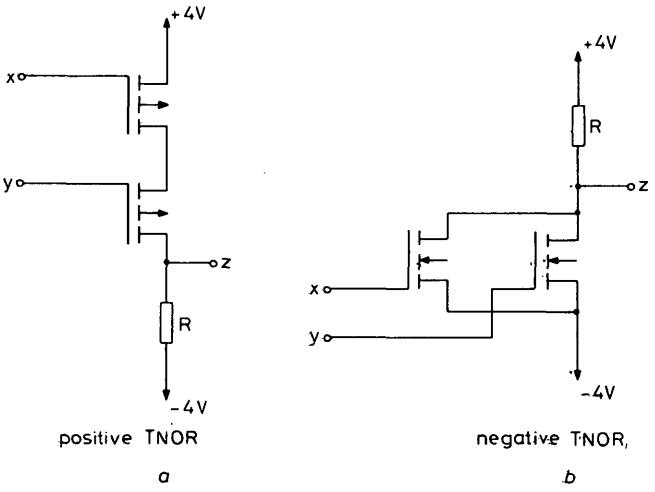

Fig. 3 *Ternary NOR circuit*
R = 25 kΩ
a Positive TNOR
b Negative TNOR

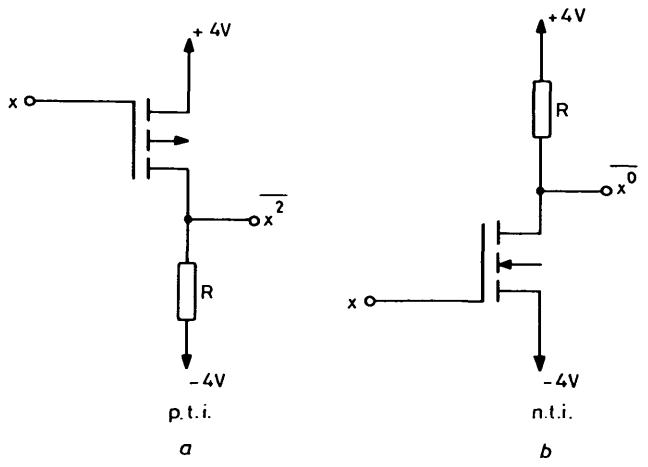

Fig. 2 *Non-complementary m.o.s. ternary inverters*
R = 25 kΩ
a p.t.i.
b n.t.i.

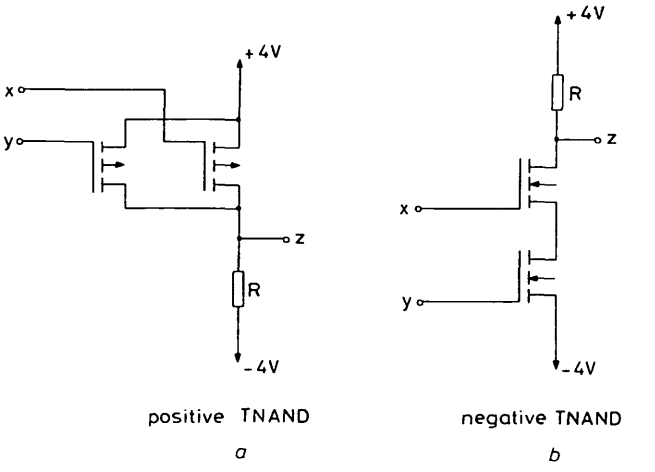

Fig. 4 *Ternary NAND circuit*
R = 25 kΩ
a Positive TNAND
b Negative TNAND

could have additional inputs beyond the two shown in the Figures.

4 Design application

Based on the ternary operator circuitry described above, it is possible to design simpler and cheaper three-valued logic systems. Examples given are for the J_k arithmetic circuit and the three-valued T-gate.

The $J_k(x)$ function[9] is defined by

$$J_k(x) = \begin{cases} 2 & \text{if } x = k \\ 0 & \text{if } x \neq k \end{cases} \quad (6)$$

where k can take the values of 0, 1 or 2.

The J_k arithmetic circuit is composed of two n.t.i., one p.t.i. and one negative TNOR connected as shown in Fig. 5. The three $J_k(x)$ functions realised are based on the following relationships:

$$J_0(x) = \overline{x^0} \quad (7)$$

$$J_2(x) = \overline{x^{2^0}} \quad (8)$$

$$J_1(x) = \overline{\{J_0(x) V J_2(x)\}^0} \quad (9)$$

The block diagram of the J_k arithmetic circuit is shown in Fig. 5*a* while its schematic diagram is given in Fig. 5*b*.

The design of the T-gate circuit is based essentially on the J_k arithmetic circuit described above. The function of the T-gate[10] is defined by

$$T(y_1, y_2, y_3; x) = y_i \quad (10)$$

where i will be equal 1 if x takes the value of 0, 2 if x is 1 and 3 if x is 2.

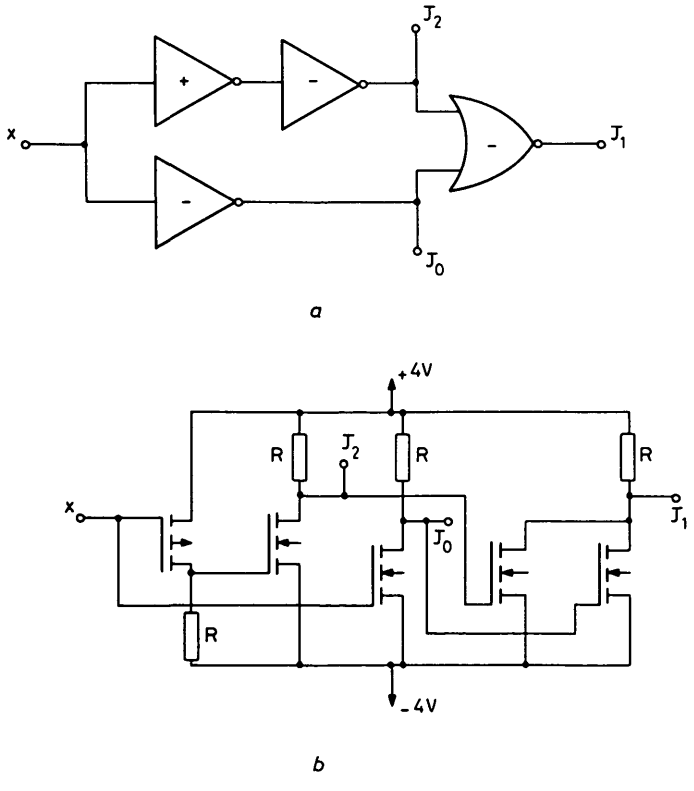

Fig. 5 *J_k arithmetic circuit*

a Block diagram
b Schematic

The block diagram of the T-gate is shown in Fig. 6. It is composed of a J_k arithmetic circuit and three ternary switches (t.s.). Each t.s. consists of one p-channel and one n-channel transistor. The source of the p-channel is connected to the drain of the n-channel and vice versa. A control signal V_c is required for proper switch operation. This signal controls the n-channel directly and the p-channel is controlled by $\overline{V_c^1}$. Both channels are biased on or off simultaneously by the control signal V_c. When V_c is equal to the high level (+ 4 V) the switch will be on, and when V_c is equal to the low level (− 4 V) the switch will be off. The J_0, J_1 and J_2 signals are connected to V_c of the t.s. that has input y_1, y_2 and y_3, respectively.

The value of x determines which of the three t.s.s will be on and, eventually, which signal (y_1, y_2 or y_3) will be displayed at the output.

Finally it should be noted that, for all circuits, all p-channel substrates are connected to the positive power supply (+ 4 V) while all n-channel substrates are connected to the negative power supply (− 4 V). All circuits presented have been realised with the commercially available MC14007 and MC14016 CMOS integrated circuits.

5 Conclusions

The use of non-complementary pairs of p-channel and n-channel m.o.s. devices in the implementation of three-valued logic circuits has been presented. This method of design reduces complexity and cost of previously reported c.m.o.s. ternary circuits by a factor of 50%. Based on the design of ternary inverters, NAND and NOR circuits presented, it is possible to configure complete three-valued arithmetic logic units which are more economical than has been previously demonstrated.

6 References

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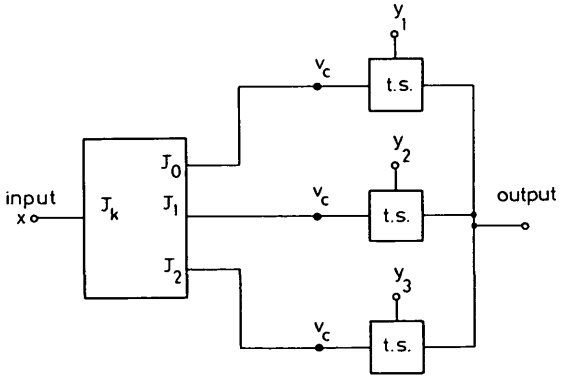

Fig. 6 *T-gate block diagram*

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