High-Speed Low-Power Adder with a New Logic Style: Pseudo Dynamic Logic (SDL)

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1 ABSTRACT

In this paper, a high speed and low power adder is designed using a new logic-design style called Pseudo Dynamic Logic (SDL). Traditional dynamic logic is pre-charged to a default value and in evaluate phase is changed to its real logic, However, in this logic style, the internal nodes are charged to an intermediate pre-charge value, so that the evaluation is performed faster.

A 32-bit CLA adder have been designed and simulated using HSPICE Level 49 parameters of a 0.6μm CMOS process. Simulated measurements on this adder show that the worst-case delay is 1.56ns. This shows 2.1 times speed improvement and 21.2% area saving in comparison to a domino dynamic logic design implemented with the same technology.

2 INTRODUCTION

Dynamic circuits are useful for designing high speed and compact circuits such as CPU [1], [4]. Dynamic logic circuits use only PDN (Pull Down Network) or PUN (Pull Up Network) of a comparable CMOS circuit, so their input capacitances and areas are reduced. The internal nodes of these logics are forced to a default value. In evaluate phase if its value is different with pre-charge value, it should be changed from VDD to VSS (or VSS to VDD) whereupon the delay is the time of this path. The other disadvantages associated with dynamic circuits are clock power [6] and died charge of node. The clock capacitance is large and the clock activity is high, so the clock power consumption is very large. The last problem is that in the pre-charge phase, charges of some nodes die. This means that they are pre-charged to predetermined values regardless of their final states.

In the following section, our proposed logic style is introduced that has smaller clock capacitance than other dynamic circuits and uses a self-timing concept. Therefore, succeeding stages can be chained together easily, and during the pre-charge phase, the charges of the internal nodes are reused.

3 SDL LOGIC

In this section, the basic operation of SDL family is described. The operation of SDL is based on Pass Gate Tree (PG) concept [2], [3]. In pre-charge phase, the previous charge stored on complementary internal node, is shared and node voltages are adjusted to an intermediate value. In evaluate phase this value changes to VDD or VSS.

Figure 1 shows a SDL gate evaluating an AND function: q = 'a'.'b'. Input variables are implemented using dual-rail signaling style. The 'ah' and 'bh' signals are equal to the input variables 'a' and 'b' respectively. 'al' and 'bl' are complimentary signals of input variables 'a' and 'b'. The Clkb is compliment of the main system clock (Clk).

3.1 PRE-CHARGE

This phase begins when Clkb is high. In pre-charge, all inputs and outputs are forced zero. N6, N7, N8, N9 and P1 transistors are 'OFF' and N1, N3 and N5 transistors are 'ON' (Figure 1).

The charges of 'qh' and 'ql' nodes are discharged from N1 or N5 respectively. The charges of 'nqh' and 'nql' are shared and voltages of 'nqh' and 'nql' nodes become about Vdd/2. N2, N4, P2, and P5 are weakly active. N2 and N4 help N1 and N5, so N1, N2, N4, N5 are weak transistors. However, the sources of P2 and P5 are floating. Therefore, these transistors do not perform any function, but partly depleting the capacitive node connected to their sources.

3.2 EVALUATE

This phase begins when Clkb is low. In evaluate phase N1, N3, and N5 are 'OFF' and P1 is 'ON' (Figure 1).

If both 'ah' and 'bh' are high, then the charge of 'nqh' is discharged through N6 (from *Vdd/2* to *Vss*) and 'nql' is charged by N9 (from *Vdd/2* to *Vdd -Vthn*) and the swing is completed to *Vdd* through P4 (whose gate is kept at a low voltage by the node nqh)

and P1. Then 'qh' becomes high and 'ql' becomes low. If 'ah' is low, then 'nqh' is charged by N7 and 'nql' is discharged by N8. If 'bh' is low and 'ah' is high, then 'nqh' is charged through N6 and 'nql' is discharged by N9. Therefore, 'qh' becomes low and 'ql' becomes high.

4 COMPLIMENT SIGNAL GENERATOR (CMPG)

If we chain this gate with another succeeding gate, the second gate should be off until evaluate phase of the first gate is completed. CMP signal shows this completion.

CMP signal is active when one of the complementary rails turns high. Figure 3 shows a simple gate that generates this signal. When Clk is low CMP becomes high and when Clk is high CMP becomes low when one of N2 or N3 turns ON. A pair of complementary signals (e.g. qh and ql) is connected to these two transistors. The next stage uses this CMP signal as Clkb.

For obtaining a better performance, the latest inputs should be connected to the node that is closer to the output.

We have proposed two chaining schemes for SDL logic. In the first scheme the gates having the same order of inputs align into one group and for each group there is one CMPG that corresponds to the slowest input of this group. In the second scheme for each gate, there is a CMPG that corresponds to the slowest input of this gate. The first scheme has area saving in comparison to the second, but the second scheme is easier to design.

5 ADDER DESIGN WITH SDL

A sample Adder was designed with Manchester carry chain (MCC) style. It has five stages (Figure 3). At the first stage, it generates 32 propagate (p_i) and generate (g_i) signals.

$$p_i = a_i \oplus b_i \quad , i=1, \ldots,32$$
$$g_i = a_i \cdot b_i \quad , i=1, \ldots,32$$

In the next stage, eight group generate (gg) and eight group propagate (gp) signals are produced for eight four-bit-wide sets of signals. 'gg' shows that at least one carry is generated and propagated to the output (e.g. C_4) and 'gp' shows that carry-in is propagated to the output (e.g. C_4):

$$gg_i = g_{i-4} \cdot p_{i-1} \cdot p_{i-2} \cdot p_{i-3} + g_{i-3} \cdot p_{i-2} \cdot p_{i-3} + g_{i-2} \cdot p_{i-3} + g_{i-1}$$
$$gp_i = C_{in} \cdot p_i \cdot p_{i-1} \cdot p_{i-2} \cdot p_{i-3}$$

In the third stage, module-four carries are produced to be used in the next stage:

$$C_0 = C_{in}$$

$$C_{4*i} = C_{4*(i-1)} \cdot gp_{(i-1)} + gg_{(i-1)}$$

At the next stage, all other carries are produced using Manchester Carry Chain (MCC) logic. At the last stage, the sum results are produced:

$$S_i = p_i \oplus C_i$$

6 ADDER SIMULATION RESULTS

We have simulated this Adder using HSPICE Level 49 models of a 0.6μm CMOS process and have measured the delay of the critical path (C_1 is generated and propagated to S_{31}), and power consumption of internal logics, input nodes, and clock tree. For a fare comparison, an optimized dynamic adder with similar blocks has been designed, optimized, and simulated. The following tables show the results of our comparative study.

6.1 DELAY

The critical path in this adder occurs when a carry is generated at the first bit and propagated to the last bit (32_{th} bit), while intermediate bits has produced no carry.

Logic Style	Tp (ns)
Dual Rail Dynamic	3.4
New SDL	1.56

Table1: Tp for the critical path.

6.2 POWER CONSUMPTION

Three components in the total power consumption are important, namely input-nodes power, internal-logic power, and clock-distribution power consumption. Input power is determined by the input capacitance. Internal-logic power consumption demonstrates two points: the internal capacitance of the gate, and short-circuit current flow. The load of the clock-distribution tree and clock activity decide the clock power consumption.

Logic Style	Input Power (mW)	Internal Power (mW)	Clock Power (mW)	Total Power (mW)
Dual Rail Dynamic	5.15	23.30	7.4	35.5
New SDL	6.20	24.13	4.4	34.73

Table2: Power Consumption.

6.3 AREA

The summation of the widths of all of the employed transistors for each circuit in each logic style gives an indication of the used area. So we use this method for area measurements, As well, total

transistor counts are given with NMOS and PMOS counts specified separately:

Logic style	PMOS		NMOS		Total Tran.
	Week	Strong	Week	Strong	
Dual rail dynamic	288	576	--	1232	2096
New SDL	288	432	720	704	2144

Table3: Number of the transistors for each adder.

Logic style	PMOS μm^2	NMOS μm^2	TOTAL μm^2
Dual Rail Dynamic	6151.68	7035.32	13187
New SDL	4769.28	5610.24	10319.52

Table4: Total area of the employed transistors.

7 CONCLUSION

An adder design with new family of dynamic logic has been introduced in this paper. In this style, charge is shared between respective internal nodes in the pre-charge phase. In the evaluate phase, if the node must turn to high, it must be changed from *Vdd/2* to *Vdd* and if it should turn to low, it must change from *Vdd/2* to *Vss*. Therefore, the speed of SDL is 2.1 times faster than dual-rail dynamic logic and has 21.2% area saving. As well, there are measurable improvements in power consumption with respect to standard dual-rail dynamic logic circuits.

8 REFERENCES

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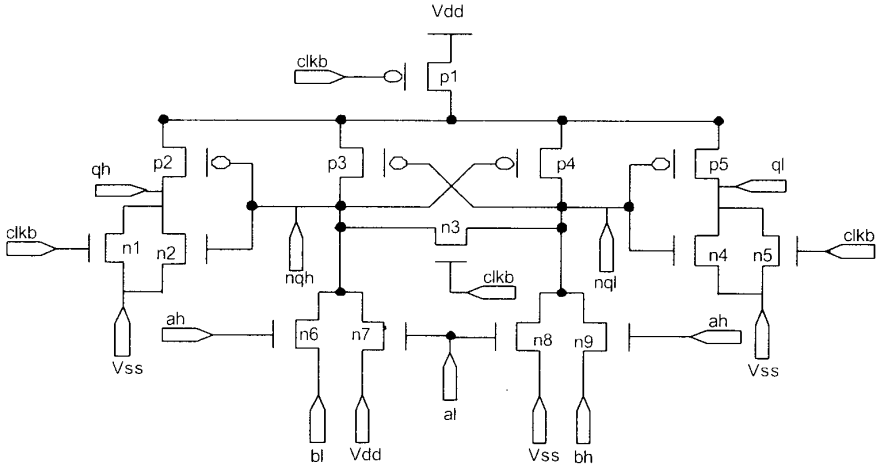

Figure 1: AND gate with SDL style.

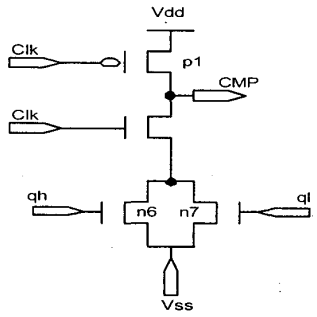

Figure 2: CMP Generator (CMPG).

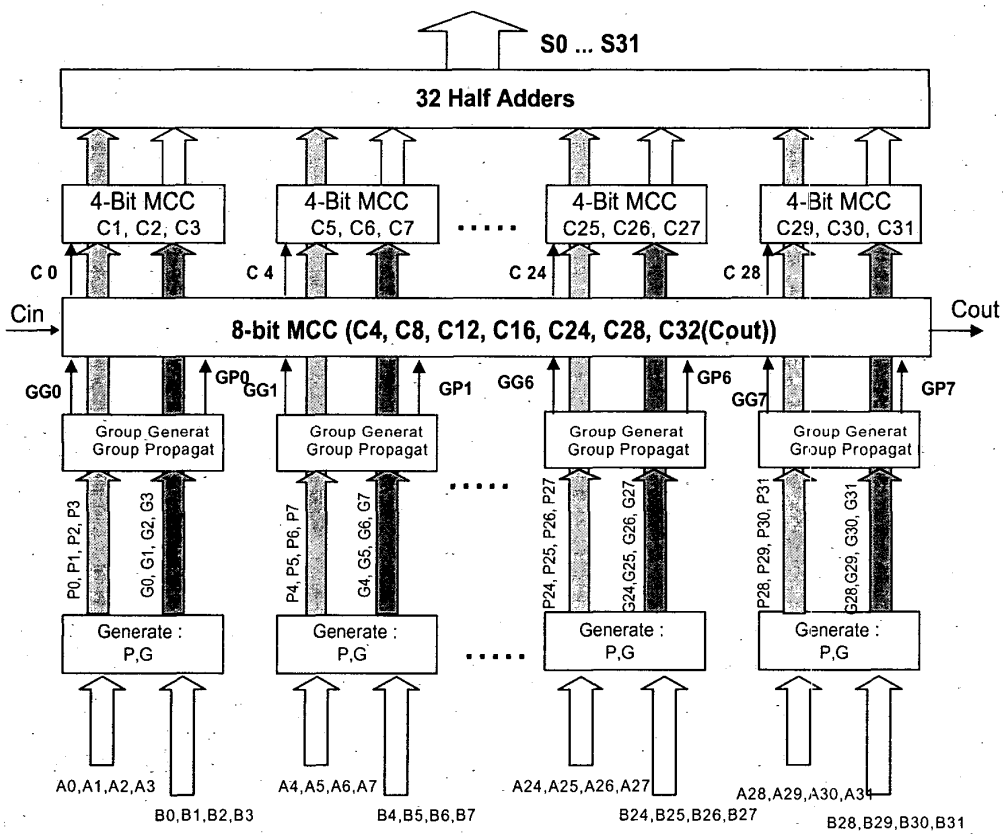

Figure 3: 32-bit Adder.