An Imager with Built-In Image-Velocity Computation Capability

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***Abstract*—An imager with built-in image-velocity computation capability is described. The image-velocity computation technique is based on signals propagating on delay lines. Silicon implementation using 3μ-CMOS technology is described. Experimental results show that a computational error of less than 20% can be achieved using currently available fabrication technology. This figure can be reduced by using larger arrays and better implementations of delay gates.**

I. Introduction

A novel image-velocity computation technique has been presented in an accompanying paper [1]. In this paper, the implementation of a velocity computing imager is reported. The velocity-computing imager implemented is intended for experimental study of the feasibility of the technique described in the accompanying paper. It can compute the velocity of a binary image only. (The light intensity inside the image boundary does not have to be even. As long as the light intensity is time invariant, the computational process will be successful even if the imager see an area smaller than the actual image area.) In the case of a real-world image or multiple moving objects are present, edge detections and image segmentations have to proceed velocity computation. Both the edge detection and image segmentation processes have been studied separately [2], [3].

II. The Image-Velocity Computing Imager

The novel image-velocity computation technique described in [1] is based on signals propagating on delay lines as indicated in Fig. 1. The delay line spacing is μ, the same as the pixel spacing. The associated delay of an element is either τ_0 or τ_1, depending on whether it is inside or outside the boundary of an image projected onto the imager. At the beginning of a computational cycle, signals enter one end of all delay lines simultaneously and propagate at a velocity μ/τ_0. In this design, the signal that propagate on the delay line is a rectangular pulse. When a rectangular-pulse signal enters the region inside the image boundary, its velocity changes from μ/τ_0 to μ/τ_1. Rectangular-pulse signals that propagate on delay lines that never intersect the image boundary propagate at a constant velocity of μ/τ_0. Analysis [1] shows that the sum of the delays of all delay lines running in the x-direction T_{2x} is

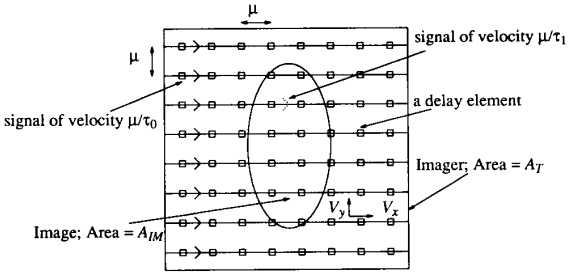

Fig. 1. The imager with built-in image-velocity computation capability.

$$T_{2x} = \frac{A_T}{\mu^2/\tau_0} + \left(1 - \frac{\tau_0}{\tau_1}\right)\frac{A_{IM}}{\frac{\mu^2}{\tau_1}[1 - (V_x\tau_1/\mu)]} \quad (1)$$

where A_{IM} is the image area, A_T is the area of the imager, and V_x is the x component of the image velocity.

To compute both the x and y components of the image velocity, a set of intersecting delay lines is required. However, using this approach to compute the image velocity requires knowledge of the image area. Moreover, without error correction, the computational error is large, even if the image velocity is low relative to the rectangular-pulse signal velocity.

Computing the image velocity without knowledge of the image area can be done using two sets of intersecting delay lines as described in [1]. In this case, the computational error is small ($< 10\%$) if the image velocity is much lower than the rectangular-pulse signal velocity ($V_x, V_y \ll \mu/\tau_1$). It has been shown [1] that if two sets of intersecting delay lines are used, the computed x component of the image velocity is given by

$$V_{xe} = \frac{(T_{2x} - T_{2xN})\frac{\mu}{\tau_1}}{T_{2x} + T_{2xN} - (2A_T/\mu^2/\tau_0)} \quad (2)$$

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where T_{2x} and T_{2xN} are the sum of delays of delay lines running in the positive x and negative x directions, respectively. An expression for the computed y component of the image velocity V_{ye} can be derived from (2) by substituting subscript y for subscript x.

Due to signal refraction at the image boundary, the computational error increases as V_x and V_y approach the V_s velocity of the rectangular-pulse signal. An error-correction scheme can be used to significantly reduce the error [1].

III. The Delay Line and Delay Summation

Delay lines have been used in the implementations of adaptive filters, decimators, and interpolators [4], [5]. In most of these applications, area is not a critical factor and synchronous delay lines are used. This allows the rectangular-pulse signal propagation to be controlled or synchronized by a global clock signal with a high degree of accuracy and stability. However, for image-velocity computation applications, the delay line must occupy an area as small as possible in order to increase the pixel density. This requires the use of asynchronous delay lines [6] having a well-controlled intrinsic delay time.

One simple approach to summing the delays of two delay lines is to cascade the two to form a longer delay line. However, for an image-velocity computing imager, the delay lines run in parallel, and an alternative method of summing the delays must be used.

The rectangular-pulse signal that propagates in the delay line is voltage mode. The difficulty of using resistors to perform on-chip voltage summation requires the conversion of the voltage signal to a current signal. Since the voltage signal is a rectangular pulse, the voltage-to-current conversion does not require a highly linear circuit. A delay line with voltage-pulse to current-pulse conversion is shown in Fig. 2(a). The output of the delay-line is connected to two cascaded inverters to generate a complementary pair of voltage signals. These signals are supplied to the input of a differential pair that acts as a switch for the tail-end constant-current source I_B.

The delay line has a delay of t_d for the positive edge of the rectangular-pulse voltage signal. When the positive edge of the rectangular-pulse voltage signal reaches the end of the delay line, transistors n_1 and n_2 of the differential pair are turned on and off, respectively. This causes the output current I_{out} of the differential pair to be equal to I_B. At the end of one cycle of operation, the input voltage of the delay line goes low. The negative edge of the rectangular-pulse voltage signal propagates through the delay line with negligible delay and reverses the differential pair. The corresponding waveform of the output current of the differential pair is shown in Fig. 2(b).

To sum the delays of all delay lines requires the summation of the output current of all delay lines and the integration of the resulting current over a fixed period by the circuit shown in Fig. 3. The MOSFET p_s acts as a switch for resetting the voltage across the capacitor C before the beginning of a new cycle. If T denotes the

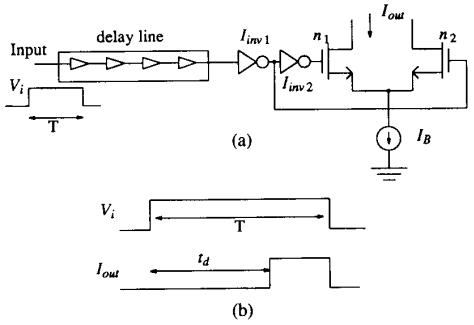

Fig. 2. The delay line and output-pulse generator.

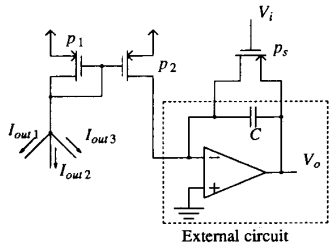

Fig. 3. The summing circuit for the output current of the delay lines.

period of a computational cycle and V_{op} denotes the output voltage of the integrator at the end of one cycle, the computed image velocity is given by [see Appendix A]

$$V_{xe} = \frac{\mu}{\tau_1} - \frac{[1 - (\tau_o/\tau_1)]A_{IM}}{\mu\left[NT - (V_{op}C/I_B) - (A_T/\mu^2/\tau_0)\right]} \tag{3}$$

where N is the total number of delay lines.

The sensitivity of V_{op} to V_x is

$$S_{V_x}^{V_{op}} = \frac{-\mu V_x\left\{NT - \dfrac{A_{IM}}{\mu[(\mu/\tau_1) - V_x]} - \dfrac{A_T}{\mu^2/\tau_0}\right\}}{A_{IM}} \tag{4}$$

where

$$NT - \frac{A_{IM}}{\mu[(\mu/\tau_1) - V_x]} - \frac{A_T}{\mu^2/\tau_0} > 0. \tag{5}$$

Equation (5) ensures that the period of computation T is long enough so that all rectangular-pulse signals have arrived at the end of their delay line before the end of a cycle of computation. Equation (5) sets an upper limit on the velocity, because if V_x is allowed to approach μ/τ_1, then the second term in (5) will increase rapidly, leading to a failure of the inequality.

It is desirable to make $S_{V_x}^{V_{op}}$ as high as possible so that $S_{V_{op}}^{V_x}$ is as low as possible. When $S_{V_{op}}^{V_x}$ is low, an error in the measurement of V_{op} will not lead to a large error in the computed V_x. There are two ways of increasing $S_{V_x}^{V_{op}}$: one is to make A_{IM} small, and the other is to make V_x large. Thus, from a practical point of view, it is easier to measure the velocity of an image with a small area pro-

vided that the image-area quantization error does not affect the computational error significantly.

IV. An Inverter with Light-Intensity Modulated Delay

The accuracy of the rectangular-pulse signal velocity depends on the delay elements used. The conventional technique of using an RC circuit to increase the delay of an inverter [7] cannot be used on a VLSI chip due to the unavailability of high-resistance resistors. An alternative technique is too narrow for image-velocity computing applications. A better technique is to use a small source-degeneration resistors to degrade the output drive capability of the inverter [8]. However, the range of controllable delays available using such a technique is to use a current source to supply (and thus to limit) the output current of the inverter [9]. This increases the time required to charge the parasitic capacitance of the output node, which thereby increases the delay of the inverter.

The schematic of an inverter with light-intensity modulated delay (in short, a *delay gate*) is shown in Fig. 4. The output-sinking current of the first inverter p_1 and n_1 is supplied by the drain currents of n_3 and n_4. The light intensity inside the image is assumed to be lower than that outside the image boundary (i.e., we are using "black" on "white" images). If the delay gate is inside the image boundary, the photodiode current is lower than the drain current of n_6. This turns off n_3 and the output-sinking current of the first inverter is supplied by the drain current of n_4 only. Recall that the rectangular-pulse signal velocity inside the image boundary should be much lower than that outside the image boundary. This can be achieved by controlling the drain current of n_4 through proper biasing. If the delay gate is outside the image boundary where the light intensity is higher, the photodiode current is higher than the drain current of n_6. The drain voltage of n_6 is then at its highest possible value. This turns on n_3 fully, with the sinking current of the first inverter being very large, limited only by n_1 and n_3. Consequently, the delay of the delay gate will be shortest and the rectangular-pulse signal velocity highest.

The function of the second inverter, p_2 and n_2, is to create a sharper transition edge for the output voltage of the delay gate. However, the input capacitance of the second inverter is amplified by the Miller effect. If the input of the second inverter is connected to the output of the first inverter directly, the changes in the Miller capacitance of the second inverter will affect the delay of the gate. This implies that the delay will be a function of the open-loop gain of the second inverter. By inserting a buffer, p_3 and n_5, between the two inverters, the input capacitance of the buffer provides a more stable load capacitance to the first inverter.

The reference voltage $V_{\text{ref}2}$, which control, the drain current of n_2, can be used to fine tune the average value of τ_1. To fine tune τ_1, the imager is first covered (implying that all delay gates are inside the image boundary). $V_{\text{ref}2}$ is then adjusted until $T_{2x} = m\tau_1$ where m is the total number of delay gates on the positive x-direction delay lines.

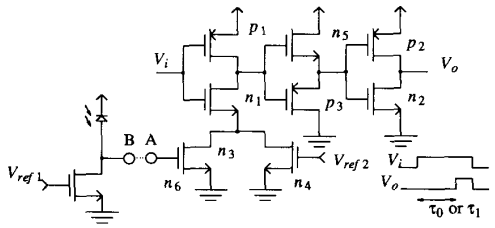

Fig. 4. The schematic of the delay gate.

V. Ground–Noise Considerations

The effect of ground noise is to produce mismatches of gate-source voltages. This causes mismatches of the delay of the delay gates. For a ground noise of 1 mV, sensitivity analysis using minimum size MOSFET shows that the contribution of the ground noise to delay mismatches is less than 2%. Thus, according to (34) of [1], the error in computed velocity due to ground noise is also less than 2%.

To reduce the effect of ground noise, either a separate ground can be provided to the source of n_4 (in Fig. 4) or a conductor of smaller sheet resistance can be used for ground. For the imager reported here, only a single ground is used. However, special attention has been paid to reduce ground noise by using wider conductors for ground, and by placing n_4 (in Fig. 4) as far away from the second inverter (p_2 and n_2) as possible. The presence of the buffer (n_5 and p_3) also helps to shield sensitive nodes from the switching noise generated by the second inverter (p_2 and n_2).

VI. Fault Tolerance and Failure Modes

To achieve reasonable image resolution, the total number of pixels should be greater than 64 by 64 or (4096) [10]. As the number of pixels increases, the delay line becomes longer, and the probability of a pixel failure increases. The imager reported here is highly fault tolerant. This results primarily from the fact that delay lines operate in parallel and the failure of one delay line will not normally affect the proper functioning of the others (unless a power-supply rail short circuit occurs). But although the failure of a single delay line will not greatly affect the overall functionality of the imager, it will increase the computational error as discussed in the following paragraphs.

There are two possible failure modes of the delay gate: the output of the delay gate can be stuck at low or stuck at high [11]. Proper functioning of the whole delay line would be destroyed if any single delay gate suffers from the first failure, that is, output stuck at low. However, the effect of this failure mode is to turn off the output current I_{out} of the particular delay line permanently. This is

equivalent to physically removing the particular delay line from the imager. Thus, the equivalent (or quantized) values of the area of both the image A_{IM} and the imager A_T, are lower.

The second possible failure mode, in which the output of the delay gate is stuck at high, will both destroy the proper functioning of the delay line and permanently turn on the output current I_{out} (i.e., $I_{\text{our}} = I_B$). However, if μ/τ_0 is very large, the effect of a failure of the second type is to remove one delay line from the area of the image A_{IM} but to leave the area of the imager A_T unchanged.

Because the effect of both failure modes is to make the quantized value of A_{IM} (i.e., A_{IMq}) lower, we can treat each such failure as an additional image-quantization error. Computational error due to image quantization has been analyzed in [1]. The result there shows that image quantization error will not significantly affect the computational error if the pixel density is high enough.

VII. Silicon Implementation and Experimental Results

A. Layout of the Imager

To experimentally evaluate the performance of the image-velocity computing imager only one set of delay lines is required. If the delay line is oriented in the positive x direction, T_{2x} can be measured by moving the image in the positive x direction. By moving the image in the negative x direction at equal speed, T_{2xN} can be measured.

A one-dimensional velocity-computing imager using the delay gate shown in Fig. 4 has been implemented using 3μ-CMOS technology. The micrograph of the image-velocity computing imager is shown in Fig. 5. Also shown in Fig. 5 is an expanded view of a delay gate (including the photodiode). The size of the array is 30 by 30 or 900 pixels. The size of a delay gate is 127.5 μm b 127.5 μm with the resulting active area (A_T) of the imager being $14.6 * 10^6$ μm^2. Except for the photodiode, all devices are shielded from light by second-layer metal. The total area of the imager including the frame and pads is 45 mm by 45 mm or $20.34 * 10^6$ μm^2. The size of each pixel will increase to 1.5 times its current size if both x-direction and y-direction lines are used.

B. Quantization Error

If the array size is not large, the velocity error due to image-area quantization will be significant. Consider the projection of a 1 mm^2 square image onto the imager described in Section VII-A. Using (12) of [1], the quantized image area associated with the positive x-direction and negative x-direction delay lines, normalized with respect to A_{IM}, are plotted in Fig. 6. As Fig. 6 shows, the quantized image area associated with the positive x-direction delay line A^+_{IMq} decays toward zero as V_x/V_s approaches 1. However, this is not the case with the quantized image area associated with the negative x-direction

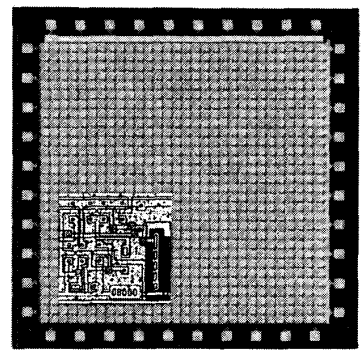

Fig. 5. The layout of the complete chip. The smaller square shows the expanded view of a pixel.

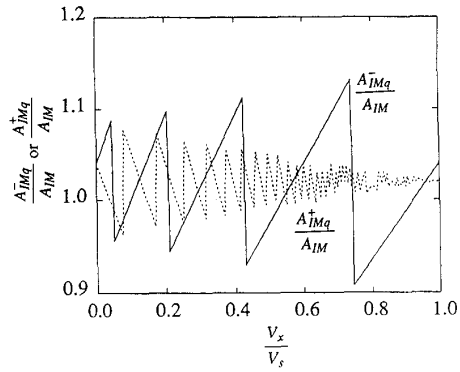

Fig. 6. Image-area quantization of an imager using one set of intersecting delay lines.

delay lines. As image velocity approaches the rectangular-pulse signal velocity, the apparent area of the image decreases. This effect increases the quantization error of the apparent area, and thus A^-_{IMq}. Close examination of (2) shows that as V_x approaches V_s (or $-V_s$), $T_{2x} \gg T_{2xN}$ (or $T_{2xN} \gg T_{2x}$). Thus, a large error in T_{2xN} (or T_{2x}) due to image-area quantization will not affect the computational error appreciably. Using (8) of [1], the velocity error as a function of V_x/V_s is potted in Fig. 7. As shown in Fig. 7, velocity errors (due to image-area quantization) of both T_{2x} and T_{2xN} approaches zero as the image velocity approaches the rectangular-pulse signal velocity. To obtain a velocity error of less than 20%, the value of V_x/V_s must be greater than 0.2. Thus, we may conclude that if two sets of intersecting delay lines are used, velocity error due to image-area quantization becomes less significant when the image velocity is comparable to the rectangular-pulse signal velocity.

C. Experimental Results

By replacing the feedback capacitor across the opamp shown in Fig. 3 with a resistor, each small step decrease in the output voltage indicates the passage of a rising edge through a delay line and its arrival at the input of the inverter $I_{\text{inv}1}$ shown in Fig. 2. This provides a means for

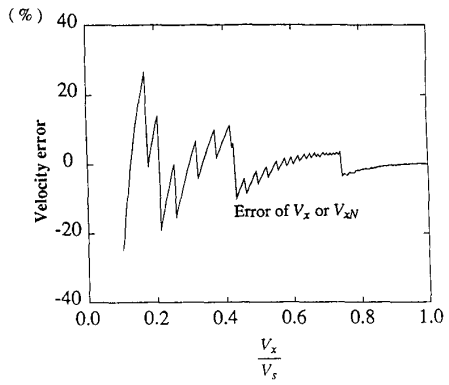

Fig. 7. Errors of V_x and V_{xN}, due to image-area quantization, when two sets of intersecting delay lines are used.

demonstrating and measuring delay-line mismatch. The results of such an experiment are illustrated in Fig. 8: when the entire surface of the imager is covered by an image, the waveform of the output voltage is as shown, completely in the lower trace, and in an expanded view in the upper trace. If all delay lines are perfectly matched, the transition edge should be a single step with a transition width of zero. In fact, from the upper trace, the width of the transition edge is approximately 15 ms. Thus, the maximum delay line mismatch is 7.5 ms. From the lower trace, the average delay of the delay line is 250 ms. It follows that the maximum delay mismatch is about 3%. This figure represents the best case. When an image of smaller area is projected onto the imager, delay mismatches are expected to be higher.

Figs. 9 and 10 show the (inverted) waveforms of the output when moving circular and moving rectangular images are projected onto the imager, respectively. Three cases are shown in Figs. 9 and 10. The velocity of the circular image is one of the following: -16000 μm/s, 0, or 16000 μm/s. The velocity of the rectangular image is one of the following: -19000 μm/s, 0, or 19000 μm/s. If a capacitor is used to integrate the output current of the delay line as shown in Fig. 3, the (inverted) waveform of the output voltage produced is as shown in Fig. 11.

A plot of the computational errors in V_x when $V_y = 0$ is shown in Fig. 12. The rectangular-pulse signal velocities inside and outside the image area used are 25,560 μm/s and 12.75 m/s, respectively. The image is rectangular with a dimension of 0.57 mm by 3.8 mm. The actual computing area of the imager A_T is 14.6 mm^2 or $14.6 * 10^6$ μm^2. Note that the errors in the computed velocities are generally small when the actual velocity is less than 18000 μm/s where $V_x/V_s < 0.7$. Above 18000 μm/s, the delay mismatch has a larger effect on the computational error due to the fact that V_x approaches μ/τ_1 (see (31), (32), and (33) of [1]), where the computational error increases significantly. Since V_y is zero, the computational error due to the refraction of rectangular-pulse signals at the image boundary is zero and no error correction is required.

Fig. 8. The output waveform for delay-gate mismatch measurement. The horizontal scales are 50 ms/div (lower) and 5 ms/div (upper) and the vertical scale is 2 V/div.

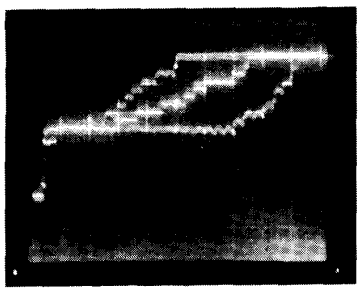

Fig. 9. The output waveform when a moving circular image is projected onto the imager. The velocity of the circular image is (left) -16000 μm/s, (center) 0 μm/s, and (right) 16000 μm/s. The vertical scale is 0.5 V/div, and the horizontal scale is 20 ms/div.

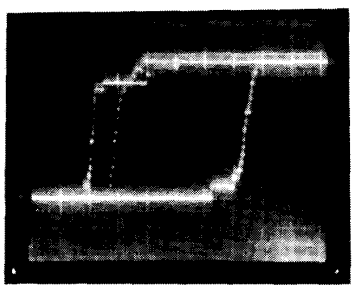

Fig. 10. The output waveform when a moving rectangular image is projected onto the imager. The velocity of the rectangular image is (left) -19000 μm/s, (center) 0 μm/s, and (right) 19000 μm/s. The vertical scale is 0.5 V/div, and the horizontal scale is 20 ms/div.

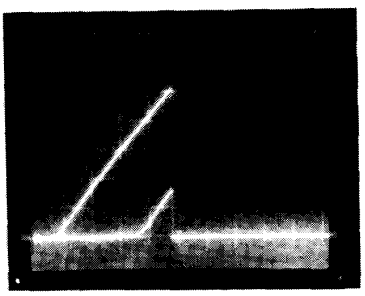

Fig. 11. The output waveform when an integrator is used to integrate the output current from the delay lines. The image velocity is -19000 μm/s (upper) and 19000 μm/s (lower). The vertical scale is 0.5 V/div and the horizontal scale is 50 ms/div.

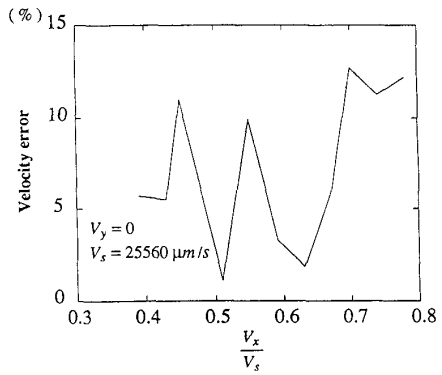

Fig. 12. The error in computed V_x when $V_y = 0$. The signal velocities inside and outside the image boundary are 25,560 μm/s and 12.75 m/s respectively. The image is rectangular with an area of 2.175 mm^2, and the computing area of the imager is 14.44 mm^2.

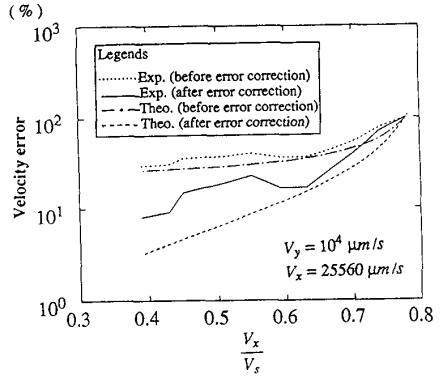

Fig. 13. The error in computed V_x when $V_y = 10^4$ μm/s.

When $V_y = 10^4$ μm/s, the computational error of V_x (before and after error corrections are performed) is shown in Fig. 13. The image used for this case is square with an area of 1 mm^2 or 10^6 μm^2. Before error correction, the computational error is generally higher than 40%. After error correction, the computational error is reduced to less than 20% for $V_x/V_s \leq 0.6$. However, for cases where $V_x/V_s > 0.7$, the error-correction scheme fails to reduce the computational error significantly. Also shown in Fig. 13 are the plots of the theoretical lower bounds (where infinite pixel density is assumed) of the velocity error before and after error correction.

The main factor that contribute to the velocity error is the small array size used. When the array is small, the number of pixels covered by any image is low. This makes the step size of the image-area quantization quite large. As a consequence, for cases where $V_x/V_s < 0.4$, the velocity error due to image-area quantization is high. However, to lower velocity error due to signal refraction at the image boundary, the imager must be operating in the range where V_x/V_s is low. Thus, it is highly desirable to reduce the velocity error due to image-area quantization. This can only be achieved by using larger arrays.

VIII. Comparison with Other Reported Techniques

Classic gradient-descent techniques are proven techniques in digital image processings [12]. Incorporating the classic gradient-descent technique into an analog velocity-computing imager requires the use of a voltage or current differentiator per pixel. These differentiators, physically distributed throughout the entire surface of the imager, have to be very well matched. Unlike the delay gate discussed here, highly random mismatches of the differentiators will not lead to error cancellation. Thus, on a VLSI chip, where process parameter variations over the entire surface cannot be guaranteed to within a few percents, analog implementations of the classic gradient-descent techniques are very difficult and good results are impossible to achieve.

One of the earliest reported analog velocity-computing imager is the correlating optical motion detector by J. Tanner and C. Mead of Caltech [13]. The technique used is similar to that used in digital image processing. A reference image frame has to be captured first. Image velocity is computed by correlating the subsequent image frames with the reference. The need for digitizer, digital storage, and the correlator leads to large amount of hardware per pixel. Generalization of this technique to 2D velocity computation will lead to impractically low pixel density. The range of computed velocity reported in [13] is much wider than that reported here. However, it is important to note that the velocity computed by the imager reported here can be increased by increasing the rectangular-pulse signal velocity.

Recently, a velocity-computing imager using delay lines to measure the time taken for an image edge to travel from one pixel to another adjacent pixel is reported [14]. Similar to that reported in [13], the imager measure only velocity of image moving in a direction parallel to a one-dimension photo-sensing array on the imager. The amount of hardware per pixel is also large and generalization of such technique to the 2D case will lead to low pixel density.

In comparison with the other velocity-computing imagers described above, the velocity-computing imager reported here has the advantage of a low transistor count per pixel and thus, a high pixel density. Accuracy of velocity computed for 1D case is comparable to that of the others. However, for 2D velocity computation, further research efforts are required to eliminate or reduce the computational errors due to delay-line mismatches and signal refractions.

IX. Conclusion

Silicon implementation of an imager with built-in image-velocity computation capability was described. Experimental results obtained show that the sources of computational error are delay-line mismatch and image-area quantization. However, as measures are taken to improve

the delay gate implementation and the IC processing technique, the ultimate limitation of this image-velocity computation technique will be image-area quantization.

APPENDIX

Refer to Fig. 3 and consider the case of one delay line only with a delay of t_d. If T is the period of one cycle of operation, I_{out} has a nonzero magnitude I_B for a time interval $T - t_d$. If I_{out} is integrated by a capacitor C the voltage across the capacitor at the end of one cycle is a function of t_d given by

$$V_c = I_B T/C - I_B t_d/C. \tag{A1}$$

Now, consider the case of N delay lines in which the output currents of the N delay lines are summed and integrated by the circuit shown in Fig. 3. By the theorem of super-position, the output voltage of the integrator at the end of one cycle is

$$V_{\text{op}} = \frac{NI_B T}{C} - \frac{I_B}{C}\sum t_d. \tag{A2}$$

Noting that $\sum t_d = T_{2x}$, (A2) becomes

$$\sum t_d = T_{2x} = NT - \frac{V_{\text{op}} C}{I_B}. \tag{A3}$$

Combining (1) and (A3) we get

$$V_{xe} = \frac{\mu}{\tau_1} - \frac{[1 - (\tau_0/\tau_1)]A_{IM}}{\mu\left[NT - (V_{\text{op}}C/I_B) - (A_T/\mu^2/\tau_0)\right]}. \tag{A4}$$

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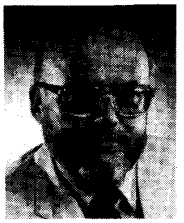

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