THREE-INPUT AMPLIFIERS

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Abstract: This paper described two novel analog-circuit-building blocks called the Three-Input AMPlifier and the Complementary Three-Input AMPlifier. These two analog-circuit building blocks find applications in data-conversion circuits.

I. Introduction

The conventional operational amplifier is acknowledged to be the most basic and versatile analog-circuit building block presently available. Such an amplifier is a single-channel device having one positive and one negative input terminal to which passive components are normally connected to construct general-purpose analog circuits. When a conventional opamp is used, the only amplifier configuration for which no passive components are required is the unity-gain buffer.

In this paper we investigate the properties of amplifier structures which have two signal channels. These amplifiers may have three or four input terminals [1]. While the four-input structure is more general than the three-input one, we find that in most important applications only three input terminals are actually employed. Consequently, we restrict our investigation to three-input structures only.

While the conventional opamp can be used to implement a unity-gain buffer without using passive components, a three-input amplifier may be used to implement a voltage summer, a voltage subtractor, or amplifiers with gains of ½ , -1 and 2, all without passive components. However, the three-input amplifier, as presently implemented, has one major drawback, namely its limited input dynamic range.

II. The three-input amplifier and its complement

The symbols and the equivalent circuits of the three-input amplifier (TIAMP) and the complementary three-input amplifier (CTIAMP) are shown in figures 1a, 1b, 2a and 2b respectively.

When negative feedback is established as shown in figures 1b and 2b, the corresponding transfer functions are respectively,

$$V_o = \frac{V_1 + \gamma V_2}{\frac{1}{A_1} + 1 + \gamma} \tag{1}$$

and

$$V_o = \frac{(1+\gamma) V_1 - \gamma V_2}{1 + \frac{1}{A_1}} \tag{2}$$

where $\gamma = A_1 / A_2$.

Under ideal conditions of $A_1 , A_2 \gg 1$ and $A_1 = A_2$, equations (1) and (2) reduce to

$$V_o = \frac{V_1 + V_2}{2} \tag{3}$$

and

$$V_o = 2 V_1 - V_2 \tag{4}$$

respectively.

Equations (1) and (2) form the basis of our analysis of the effects of channel mismatch ($A_1 \neq A_2$), finite open-loop gain, and finite open-loop bandwidth.

If $A_1 = A_2 = A$, a finite value, the ideal transfer functions, expressed by equations (3) and (4), are scaled by constant factors given by $2A / (1 + 2A)$ and $A / (1 + A)$ respectively. Thus, the closed-loop-gain errors of the TIAMP and CTIAMP are,

$$\varepsilon(TIAMP) = \frac{1}{1+2A} \tag{5}$$

and

$$\varepsilon(CTIAMP) = \frac{1}{1+A} \tag{6}$$

To study the effect of finite open-loop bandwidth, we replace A by $A = \omega / j\omega$. It follows from equations (1) and (2) that

$$\omega_{3dB}(TIAMP) = 2\ \omega_u \tag{7}$$

and

$$\omega_{3dB}(CTIAMP) = \omega_u \tag{8}$$

The transfer functions expressed by equations (1) and (2) may also be implemented using conventional operational amplifiers (opamps) and a few resistors as shown in figures 3 and 4 respectively. If we compare equations (5), (6), (7) and (8) with the corresponding equations for the circuits shown in figures 3 and 4, the following conclusions can be drawn:

> (*i*) For equal dc open-loop gains, the closed-loop-gain errors of the TIAMP and CTIAMP are approximately half those of their counterparts implemented using conventional opamps.
> (*ii*) For equal open-loop bandwidths, the closed-loop 3dB-bandwidth of the TIAMP and CTIAMP are twice those of their counterparts implemented using conventional opamps.

While the closed-loop-gain error may be affected by a finite open-loop gain, the dominant cause of closed-loop-gain error is channel mismatch. If we assume that $A_1 \neq A_2$ and $A_1 , A_2 \gg 1$, from equations (1) and (2) we may deduce that for both TIAMP and CTIAMP, the closed-loop-gain errors are $1-\gamma$ and the input voltage V_2 is scaled by a factor γ. Generally, mismatch of the two channels may be a function of input-signal frequency. However, for circuit implementations of the TIAMP and CTIAMP with a single dominant pole, it can be shown that the two channels are matched over the input-frequency range as long as the dc open-loop gains of the two channels are equal.

III. Circuit implementation of the three-input amplifier

To simplify our discussion, consider the simple implementation of the TIAMP shown in figure 5. More practical circuits using cascode configuration will be discussed subsequently. Note that by changing the connections between the drains of N_1, N_2 and P_2, P_4 to the drains of P_1, P_3, the schematic is converted into that of the CTIAMP.

The operating principle of the TIAMP can be best described by assuming the tail-end biasing currents of the two differential pairs to be equal, and the gain of the second stage (N_3 and P_7) to be infinite. When two input voltages V_1 and V_2 are applied to the positive input terminals, and the output voltage is applied to the negative input terminal to establish a negative feedback, the output current of the input stage is the difference of the drain currents of P_2 and P_4, that is $i_o = I_{ds4} - I_{ds2}$. Since the second stage has infinite gain, in the presence of negative feedback, i_o must be zero. It follows that $I_{ds2} = I_{ds4}$. Since the tail-end biasing currents of the two differential pairs are equal, the drain currents of P_1 and P_3 must also be equal, $I_{ds1} = I_{ds3}$. Therefore, current tracking occurs within the input stage of the TIAMP. If the transistors are ideal, equal voltage drops across the inputs of the two differential pairs are required to produce the current tracking discussed earlier. This requires $V_1 - V_o = V_o - V_2$ or $V_o = (V_1 + V_2) / 2$; a situation which is termed "voltage averaging".

Small-signal analysis shows that for the two channels to be matched, the following conditions should be observed,

$$g_{mp1} \,||\, g_{mp2} = g_{mp3} \,||\, g_{mp4} \tag{9}$$

and

$$g_{mn1} = g_{mn2} \,. \tag{10}$$

The dominant pole of the circuit is at

$$P_1 = -\frac{(g_{op7} + g_{on3})(g_{op4} + g_{on2})}{C_c\, g_{m3}} \tag{11}$$

and this pole is common to both channels.

IV. Channel matching in the TIAMP

Mismatch of the two channels can occur only within the input stage. Analysis of the input stage leads us to

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$$V_1 + V_2 - 2V_o = \varepsilon_1 + \varepsilon_2 \tag{12}$$

where

$$\varepsilon_1 = \left(|V_{Tp2}| - |V_{Tp1}| \right) - \left(|V_{Tp4}| - |V_{Tp3}| \right) \tag{13}$$

and

$$\varepsilon_2 = \left\{ \left[\frac{2I_{dsp2}}{k_{p2}} \right]^{1/2} + \left[\frac{2I_{ds3}}{k_{p3}} \right]^{1/2} \right\} - \left\{ \left[\frac{2I_{dsp1}}{k_{p1}} \right]^{1/2} + \left[\frac{2I_{dsp4}}{k_{p4}} \right]^{1/2} \right\} . \tag{14}$$

Ideally, the error terms ε_1 and ε_2 should be zero.

If the intrinsic threshold voltages of P_1 to P_4 are equal, according to equation (13), ε_1 will remain zero for any changes in V_T due to body effect because the source-bulk voltages of P_1 and P_2, P_3 and P_4 are equal. It follows that any mismatch of the two channels is mainly due to ε_2.

The effects of nonidealities, such as transconductance mismatch in the current mirror and the differential pairs, are determined using equation (14). The results are summarized as follows:

(i) If $k_{p1} = \varepsilon_p\, k_{p3}$ and $k_{p2} = \varepsilon_p\, k_{p4}$,

$$\varepsilon_2^{i} = \sqrt{2} \left[1 - \left(\frac{1}{\varepsilon_p} \right)^{1/2} \right] \left\{ \left[\frac{I_{ds} - I_{dsp4}}{k_{p3}} \right]^{1/2} - \left[\frac{I_{dsp4}}{k_{p4}} \right]^{1/2} \right\} \tag{15}$$

where $I_{dsp5} = I_{dsp6} = I_{ds}$.

(ii) If $I_{dsp5} = I_{dsp6} + \varepsilon_{Id}$,

$$\left(\varepsilon_2^{ii} \right)^2 \simeq \frac{2}{k_p}\, \varepsilon_{Id} \tag{16}$$

where $k_{p1} = k_{p2} = k_{p3} = k_{p4} = k_p$.

(iii) If $I_{dsn2} = I_{dsn1}\,(1 - \varepsilon_{mm})$,

$$\left(\varepsilon_2^{iii} \right)^2 \simeq 4\, \frac{I_{dsp2}}{k_p} \left\{ 1 - \sqrt{1 - \varepsilon_{mm}} \right\} \tag{17}$$

However, the effect of mismatch in the current mirror may be made negligible, if the drains of P_1 and P_3 are connected to the drains of P_4 and P_2 respectively, to form a more symmetrical configuration.

(iv) If the gain of the second stage is not infinite but is given by A_{m2},

$$\left(\varepsilon_2^{iv} \right)^2 \simeq \left(\frac{4}{A_{m2}\, k_p} \right) V_o \tag{18}$$

on the assumption that $I_{dsp3}, I_{dsp4} \gg i_o$, where i_o is the output current of the input stage.

ε_2^{ii} is a constant, and causes only an output offset voltage, while ε_2^{iii} can be reduced so as to be negligible. Therefore, channel mismatch is dominantly due to ε_2^{i} if A_{m2} is reasonably large. If we assume $k_{p3} = k_{p4}$ in equation (15), ε_2^{i} is zero if $I_{ds} = 2I_{dsp4}$, that is $V_i = 0$. However, as V_i approaches its positive or negative limits, I_{dsp4} approaches I_{ds}, or zero, which leads ε_2^{i} to approach its maximum magnitude. As will be discussed in the following section, second-order effects in the MOSFETs also cause the greatest channel mismatch when V_i approaches its theoretical limits.

Similar analysis of the schematic of the CTIAMP yields the same results as those for the TIAMP.

V. Consideration of second-order effects

While short-channel modulation and other second-order effects in MOSFETs reduce the CMRR and open-loop gain of the conventional opamp, the same second-order effects may cause significant channel mismatch in the TIAMP. In this section, analysis using a more accurate MOSFET model described elsewhere [2] is performed.

Transconductance mismatches between the differential pairs have been shown to be the dominant cause of channel mismatch in the TIAMP in the previous section [equation (15)]. The transconductance mismatch of the transistors may be due to different aspect ratios (a random error) or due to second-order effects in the transistors (a systematic error). A non-zero input voltage causes unequal drain-source voltages in all input transistors. The drain-source voltage of P_4 (in figure 5) has the largest variation due to its large load impedance. The effect of drain-source voltage on the transconductance of the transistor can be understood as follows:

We may write

$$k = \frac{W}{L} \left(\frac{\mu C'_{ox}}{1 + \delta} \right) \tag{19}$$

It follows that

$$\frac{\delta k}{\delta V_{ds}} = \frac{W\, C'_{ox}\, \mu\, \theta\, (1 - \delta)}{2L\, (1 + \delta)\, (1 + \theta f_u)} \tag{20}$$

where the definitions of the symbols can be found in [2]. In deriving equation (20) we have omitted the short-channel-modulation effects which only worsen the effect of V_{ds} on k.

Close study of equation (20) shows that the maximum value of $\delta k / \delta V_{ds}$ occurs when f_u reaches its minimum value under the condition

$$V_{gs} = V_T \ . \tag{21}$$

It follows that the maximum transconductance mismatch occurs when one transistor in a differential pair is approaching the turn-off region of operation. This corresponds to the case when the input voltage approaches its maximum allowable value. Thus, closed-loop gain errors for large input voltages are dominantly due to the transconductance mismatch in the differential pairs. However, this mismatch may be reduced by increasing the biasing currents of the differential pairs so that no transistor in the differential pair is close to turn-off when the input voltage reaches its maximum allowable value. But, large biasing currents lead to large gate-source voltages for P_1 to P_4, and reduce the drain-source voltages of the two transistors supplying the tail-end biasing currents. This not only causes a reduction in the open-loop gain, but also leads to a mismatch of the tail-end biasing currents by increasing the sensitivity of the channel lengths of the biasing-current transistors to their drain-source voltages. This is illustrated by the following analysis:

By differentiating ΔL (given in [2]) with respect to V_{ds}, we get

$$\frac{\delta \Delta L}{\delta V_{ds}} = \frac{\left[2\, \varepsilon_s / q\, N_A \right]^{1/2}}{2 \left[\phi_d + \left(V_{ds} - V'_{ds} \right) \right]^{1/2}} \ ; \ V_{ds} > V'_{ds} . \tag{22}$$

Thus, $\delta \Delta L / \delta V_{ds}$ reaches its maximum value when $V_{ds} = V'_{ds}$ or, equivalently, when the transistor approaches its triode region of operation.

In a conventional opamp, the short-channel-modulation effect degrades the output-impedance of the biasing-current source and causes a reduction in CMRR. However, in the TIAMP, due to the difference in the drain-source voltages of the two transistors providing the tail-end biasing currents, such an effect causes a biasing current mismatch. Thus, a larger value of $\delta \Delta L / \delta V_{ds}$ will produce a larger mismatch in the tail-end biasing current. For this reason, a TIAMP using p-type differential pairs has a more linear transfer curve for relatively negative input voltages. Correspondingly, an n-type pair functions best for positive input voltages.

From the above, we may conclude that large tail-end biasing currents will produce transfer curves that are more linear at the lower (upper) end if p-type (n-type) differential pairs are used. However, small tail-end biasing currents will produce a transfer curve that is more linear around the origin.

Silicon implementations

Three designs of the TIAMP and CTIAMP, shown in figures 5, 6 and 7, have been fabricated at Northern Telecom under the auspices of the Canadian Microelectronic Corporation using 3μ-CMOS technology. The layouts of the three versions of the design are shown in figures 8, 9 and 10, respectively.

The second version was fabricated to study the effect of connecting the drains of P_1 and P_3 to the drains of P_4 and P_2 respectively. The third version, which has a folded-cascode input stage, eliminates the unbalanced output impedances seen by the differential pairs, to improve the linearity of the transfer function. The areas of the three versions of the design are 0.12 mm^2, 0.12 mm^2 and 0.17 mm^2 respectively.

For each version of the design, there are five fabricated amplifiers available. This results in a total of thirty amplifiers available for testing. Of the thirty amplifiers, one (version 3 of TIAMP) was found to be non-functioning. This indicates a percentage yield of approximately 97%.

For a peak-to-peak input-voltage swing of 2V, the closed-loop-gain errors of the three versions of the TIAMP are less than 1%, 0.4% and 0.4% respectively. For the CTIAMP, the corresponding figures are less than 1.25%, 0.25% and 0.23% respectively, for a peak-to-peak input-voltage swing of 1V. When the inputs of version three of TIAMP and CTIAMP are excited by a sine-wave at 10 kHz, the measured output waveforms are as shown in figures 11 and 12 respectively.

The closed-loop 3dB frequencies of the TIAMP are 5.1 MHz, 4.3 MHz and 1.3 MHz respectively. The corresponding figures for the CTIAMP are 3.7 MHz, 3.3 MHz and 1.4 MHz respectively. [1] The wide 3dB-bandwidths lead to short settling times. For the TIAMP, the settling times have been

[1] The compensation capacitors in the TIAMP and CTIAMP are not equal; therefore, the corresponding ω_u are also not equal.

measured to be 1 μs, 1.5 μs and 2 μs respectively, with load capacitances less than 50pF. The corresponding figures for the CTIAMPs are 0.9 μs, 1.6 μs and 5 μs respectively. The output waveforms of version one of the TIAMP and CTIAMP, when excited by an input step-voltage, are shown in figures 13 and 14 respectively.

Experimental and simulated results are summarized in Table 1. Both sets of results agree fairly well except for ω_{3dB} of version two of the TIAMP. Generally speaking, simulation results tend to deviate from the experimental results when a resistor is used to reduce the feedforward provided by the compensation capacitor. This is because the tolerance of the value of the resistor on the chip can be as large as 50%.[2]

VII. Conclusion

This paper has described two new types of amplifiers. The three-input amplifier may be configured directly to have a gain of one half and may also be used as a voltage summer. The complementary three-input amplifier may be configured directly to have gain of two or of negative one. The three-input amplifier is useful in the area of D/A conversion [3, 4, 5] while the complementary three-input amplifier is suited to a role in A/D conversion [3, 6].

Three versions of the three-input amplifier and its complement have been fabricated. Experimental results have confirmed the characteristics of the amplifiers as predicted by theoretical analysis.

VIII. Acknowledgement

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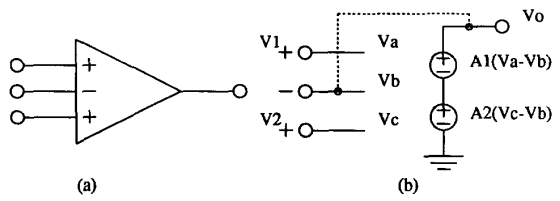

Figure 1: (a) The three-input amplifier and (b) its equivalent circuit

[2] The effect is particularly pronounced when the resistor value is chosen to minimize t_s and maximize ω_u.

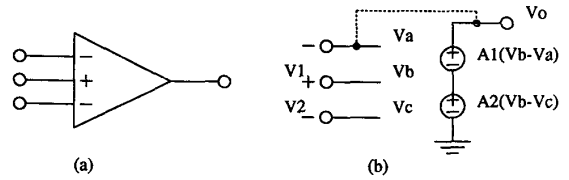

Figure 2: (a) The complementary three-input amplifier and (b) its equivalent circuit

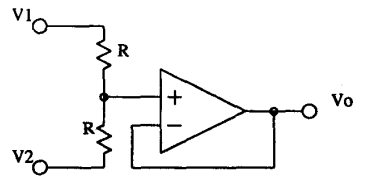

Figure 3: A voltage summer implemented using a conventional operational amplifier

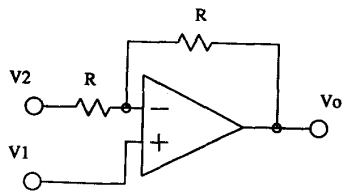

Figure 4: A voltage subtractor implemented using a conventional operational amplifier

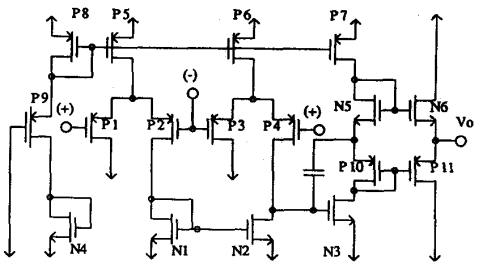

Figure 5: A possible implementation of the three-input amplifier

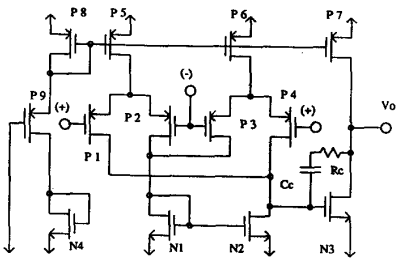

Figure 6: The second version of the three-input amplifier design

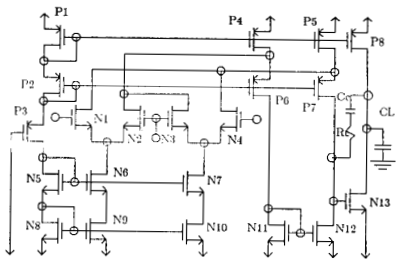

Figure 7: The third version of the three-input amplifier design

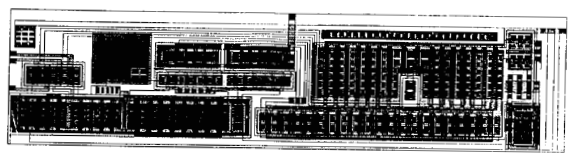

Figure 8: The layout of the version 1 of the three-input amplifier

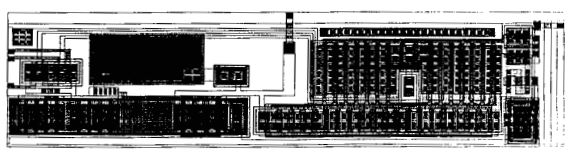

Figure 9: The layout of the version 2 of the three-input amplifier

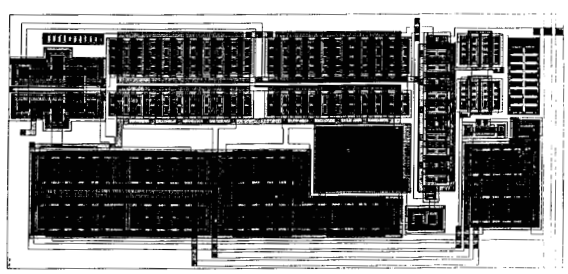

Figure 10: The layout of the version 3 of the three-input amplifier

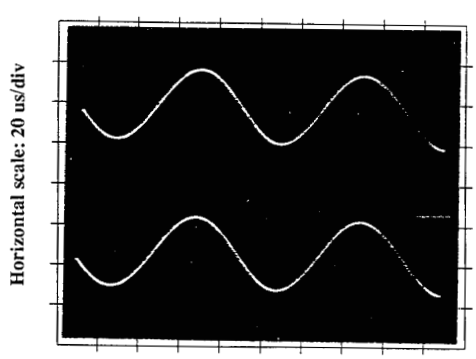

Figure 11: The output waveform of version 3 of the three-input amplifier: The upper trace is the output waveform (0.5V/div) and the lower trace is the input waveform (1V/div)

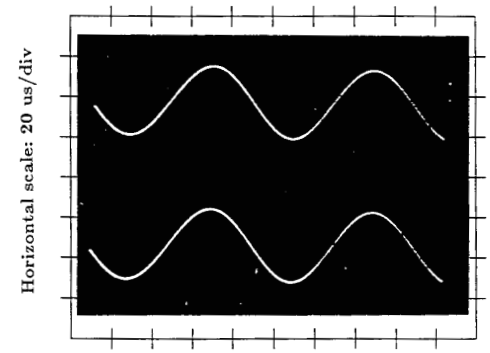

Figure 12: The output waveform of version 3 of the complementary three-input amplifier: The upper trace is the output waveform (1V/div) and the lower trace is the input waveform (0.5V/div)

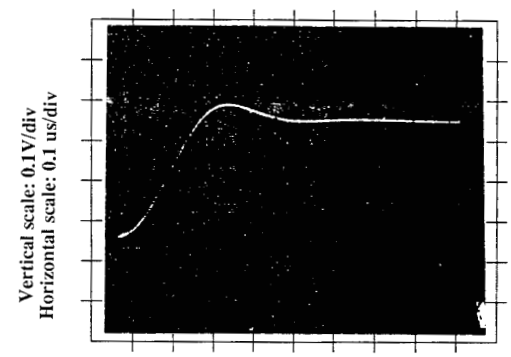

Figure 13: The step response of version 1 of the three-input amplifie

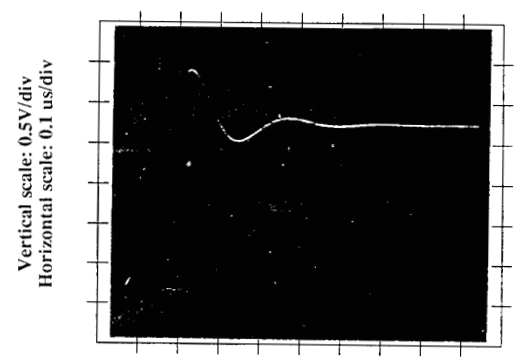

Figure 14: The step response of version 1 of the complementary three-input amplifier

TIAMP	VERSION 1	VERSION 2	VERSION 3
ω_{3dB}	5.0 MHz	6.0 MHz	1.4 MHz
$\omega_{3dB}(meas.)$	5.1 MHz	4.3 MHz	1.3 MHz
t_s	1.1 μs	1.4 μs	2.1 μs
$t_s(meas.)$	1.0 μs	1.5 μs	2.0 μs
CTIAMP	VERSION 1	VERSION 2	VERSION 3
ω_{3dB}	4.0 MHz	3.2 MHz	1.5 MHz
$\omega_{3dB}(meas.)$	3.7 MHz	3.3 MHz	1.4 MHz
t_s	0.8 μs	1.6 μs	5 μs †
$t_s(meas.)$	0.9 μs	1.6 μs	5 μs †

Table 1: Simulated and measured 3dB-frequencies and settling times (for a load capacitance of 50 pF and 0.1% error)

† for a load capacitance of 20 pF.