SWITCHED CAPACITOR CIRCUITS IN THE IMPLEMENTATION OF MULTIPLE-VALUED LOGIC

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ABSTRACT

The discretized-analog nature of switched-capacitor(SC) technology has not been associated with multiple-valued logic (MVL) designs in any publication heretofore. In this paper, the possibility of employing SC technology for MVL circuit implementation is investigated, and attendant potential benefits are discussed. The circuit design of a novel SC MVL multiplier is proposed, and the direct realization of general MVL functions by combining SC technology and pass-transistor structures is presented.

1. INTRODUCTION

Multiple-valued-logic circuit designs exist in various technologies and in different modes of operation (current, charge, voltage or some hybrid combination). Each has its advantages and disadvantages. However, to the authors' knowledge, MVL circuit designs using SC technology have yet to be proposed, or at least, have never been reported. The closest conventional equivalent appears in CCD technology.

Using capacitors, which are charged and discharged periodically to emulate the action of resistors, SC technology has successfully eliminated the need for explicit resistors in analog filter designs. Thus, for VLSI implementation, SC technology makes analog filters small, precise and quite convenient. SC technology has also been employed for non-filtering applications such as in A/D converters [1], analog multipliers [2], rectifiers [3], and oscillators.

However, in spite of its popularity in diverse applications, the discretized-analog nature of SC has not yet been exploited for MVL circuit implementation. Perhaps this is because it is true that SC technology has certain shortcomings: SC is intrinsically slower than conventional digital technologies [4]. Its major component, the op amp, is large (relative to a logic gate) and not subject to dimensional scaling as easily as a binary gate. Nevertheless, SC has its own merits: As a quantized analog technique, it has a natural affinity to multivalued applications. It consumes low power, a property which is essential for VLSI implementation. It incorporates abundant low-cost memory which makes multiplexing and the use of cyclic schemes quite feasible [5]. As well, no resistors are involved, as they are in most MVL voltage-mode designs. Circuit fan-out is not limited to one as it is in CCD schemes. Charge summing is not much more difficult than the direct wiring connection used for current summing. Moreover, the rather low speeds of SC operations are not always a concern if the target application does not demand high-speed operation. Furthermore, by multiplexing, op amps can be re-used and the numbers of op amps can be reduced [5]. Another fact is that the requirements (settling time, internal noise, dc offset, etc) on op amps for use in MVL circuits are not as stringent as those on op amps used for other purposes (such as in SC analog filters or A/D converters). This relaxation of requirements will result in simpler designs for op amps for MVL applications. Thus, as technology advances, it might be possible to reduce significantly the size of op amps suited to MVL.

To demonstrate the natural relationship of SC to MVL, a fixed-point MVL SC multiplier has been designed. The SC MVL-multiplier design considered here aims at low-speed applications such as audio filtering. In order to illustrate and exploit the base-independent characteristic of SC, base 8 has been targeted. This, as well, is in marked contrast to the normally lower base values required by other technologies.

To demonstrate the more general flexibility of SC techniques, a combined SC and pass-transistor approach has also been explored. It is shown that by combining pass-transistor structures with SC circuits, better designs, in terms of performance, power consumption and circuit simplicity, may result.

2. MVL SIGNAL CREATION, DETECTION, AND RESTORATION

General speaking, in MVL circuit designs, signal creation, detection and restoration are not the simple tasks they are in binary logic. Efficient designs for any of these particular circuit functions may make a particular implementation scheme attractive. On the other hand an over-complicated structure for any of these functions will make the proposed scheme uncompetitive. Therefore, the study of the implementation of the three basic functions is very important.

To set the stage for a presentation of SC alternatives, we will first review the properties of available techniques, and in particular those in voltage, current and charge modes.

2.1. Voltage Mode

In voltage-mode circuits, signal detection is performed by one of three methods. They are:

(1) Comparison with logic-rail references either in the form of distributed MVL reference buses or locally-generated voltages using a voltage divider, perhaps employing a stack of diode-connected transistors.

(2) Using the threshold of an MOS transistor as a reference. A wide range of MOS thresholds can be attained by ion implantation.

(3) Using device-size-adjusted thresholds of inverters. The threshold of a simple inverter can be adjusted by varying the W/L ratios of its MOS transistors, or by stacking MOS devices having the same W/L ratio.

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Signal creation and restoration are usually done by summing the outputs of the threshold detectors which are used for signal detection. Summation is performed by an adder normally comprising an amplifier and suitably weighted resistors.

Most voltage-mode circuit schemes use resistors and are thereby unsuited to VLSI implementation. Furthermore, the schemes are usually restricted to low-base-value applications.

2.2. Current Mode

Current-mode circuits are generally much superior to voltage-mode ones. Signal detection is typically done by feeding an input current to a current mirror which is biased by a weighted current source. The high output impedances of the weighted current source and the current mirror ensure a high sensitivity in the process of current-to voltage conversion and thus a sharp detection threshold.

Signal provision and restoration are performed by simple direct-wire summing. The simplicity of the current-mirror, which has become the basic unit in current-mode circuits, makes current mode very attractive for MVL design.

While it is true that current-mode circuits can be employed to achieve area reduction, high-speed operation and simplicity of circuit structure, they still have some drawbacks. These include high power consumption and a lack of the low-cost memory which is essential for sequential circuits. Furthermore, as the base value increases, a wider range of logic values requires a wider range of MOS sizes. Unfortunately at the same time, large MOS transistors bring undesirable effects to the static and dynamic behavior of otherwise simple circuits.

2.3. Charge Mode

Existing charge-mode MVL circuits are solely CCD circuits. There are generally four MVL basic-gate types in CCD implementations. They are Constant, Addition, Fixed Overflow and Inhibit [6]. The corresponding basic functions, as the names of these gates imply, are charge creation, charge addition, charge overflow and conditional charge transfer.

Signal detection is provided using a combination of Fixed Overflow and Inhibit. Fixed overflow allows charge to spill through weighted storage gates and therefore to provide multiple-threshold references. Inhibit provides a sharp detection of whether or not there is certain amount of charge in the corresponding well of a storage gate.

Signal provision and restoration are done using the Addition gate which sums up the results and supplies output.

The high packing density that makes CCD literal gates small and inexpensive, the low power consumption and MOS compatibility which enhance VLSL implementation, and the base-value-independent nature of CCD technology, have all contributed to the superority of CCDs in a particular domain of MVL circuit design. Nevertheless, the CCD approach is not perfect. Its weaknesses include limitations in speed and fan-out. In particular for a relatively higher base value, larger packets of charge have to "fill and spill" through more storage wells and this results in even slower operation. Allowing certain amount of residual charge can increase speed, compensating for the fact that each remaining elemental charge takes proportionally longer to transfer. However, this approach provides a particular problem in high-radix systems. For example, in a radix-10 system, 5% of a logic signal 9 is almost half of the minimum logic separation!

Thus one can see that all existing technologies and circuit schemes have their respective strengths and weaknesses for MVL implementation. As a consequence, any new technology or design scheme that can overcome some of the many possible limitations is worthy of investigation, even though it may not appear superior in other respects. In the authors' view, SC technology is such a case.

2.4. SC Technology

SC is actually a hybrid-mode technology, for charge-to-voltage conversion and its inverse frequently occur during signal processing. Therefore, it may conceivably be arranged to combine some of the advantages of voltage-mode circuits with some of those of charge-mode circuits, if manipulated properly.

There are a few well-developed basic SC building blocks. They are integrators, adders (or subtractors), gain stages or buffers and comparators (figure 1). In the diagrams, an "X" represents a switch and the number besides it indicates the clock phase during which the switch is closed. These circuit blocks all have very similar structures. In fact some of them have exactly the same topology but use different clock signals, or rather, use the same clock signals arranged in a different sequence.

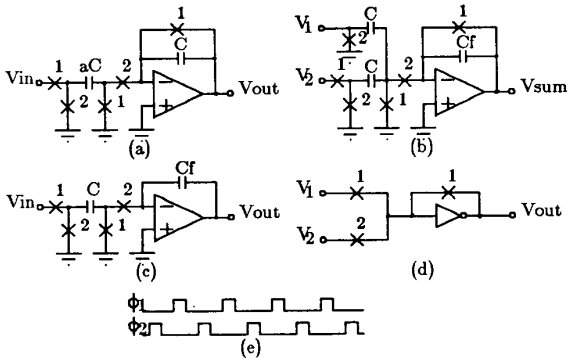

FIG 1 (a) Gain Stage, (b) Adder, (c) Integrator, (d) Comparator, (e) Clock signals

Since SC is a hybrid-mode technology, MVL-signal detection can also be performed by one of two means, namely voltage comparison or charge subtraction.

For voltage comparison, the required voltage references can be provided by MVL buses or generated locally as is done for normal voltage-mode circuits. However, an important difference occurs when the voltage references are allowed (or required) to step down or step up sequentially. This incremental operation is extremely simple to achieve using an SC integrator. In fact, the resulting circuit is no more complex than the SC gain stage that is required to generate a single voltage reference. Of course, such is not the case for normal voltage-mode circuits.

Alternatively, the charge-subtraction method uses a constant voltage reference, normally the power supply, to charge up a weighted capacitor whose calibrated charge will be subtracted from the input charge. The result is compared to a fixed reference. The idea is illustrated by the threshold detector shown in figure 2, where the factor a is a weight between 0 to 1 and is also the threshold value expressed as a fraction of the supply voltage.

Which of the 2 detection schemes suggested above should be used? The answer depends on the complexity of the corresponding circuits. If signal detection against the same threshold is required at many points in a circuit, voltage comparison would be more desirable. This follows, since the overhead of a single voltage reference generator is well-compensated by the component-count reduction of several relatively more complex charge-subtraction detectors. On the other hand, the charge-subtraction method would be better if the situation is reversed.

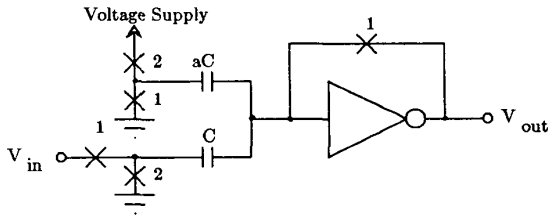

FIG 2 Charge-Subtraction Threshold Detector

Provision of MVL signals is usually done by adders similar in effect to the Addition gate in CCDs. However, while an SC adder can be considered to accept either voltage or charge as input, the output is always a voltage signal obtained at the output of an op amp. Therefore, unlike the situation in CCDs, this output exhibits low impedance and is capable of driving a number of gates.

Signal restoration can be effected by using a number of threshold detectors selected from one or the other of the 2 schemes, and an SC adder which sums up the outputs of the detectors. This idea is not unique to SC implementation; it is also commonly used in other technologies: In fact it is equivalent to a binary flash A/D-converter pair. Note that subranging or pipelined structures could be applied here to reduce the circuit size while maintaining signal throughput.

Some restoration-circuit schemes which are unique to SC technology will now be introduced:

(1) The first scheme is the cyclic A/D converter pair (figure 3) [1]. It is particularly suited for SC implementation because of the availability of low-cost memory. This scheme does not require widely-distributed logic rails. Neither does it induce a wide spread of capacitor values as is required for the charge-subtraction detection method. However, it can conveniently deal only with base values which are powers of 2. Otherwise, additional voltage references and a larger capacitance spread are inevitable. Another drawback is that a number of cycles ($\log_2 R$, where R is the base value) are required to complete a single restoration. Precision is also a problem because the input signal must travel through several stages, and in each there will be accumulating error. To reduce the accumulated error, a refreshing-reference scheme proposed by Cheung-Chung Shih [1] allows both the signal and the reference to travel through the same path. Note that the cyclic structure can be stretched into a pipelined structure to increase throughput rates at obviously higher cost.

(2) The second method can be called the step-integration method. It requires no logic rails, and has a satisfactory speed. This method uses two SC MVL counters, one up-counter and one down-counter, with two comparators. The MVL input signal is simultaneously compared to the outputs of both counters. As soon as either one of the comparators changes state, counting will be stopped and a constant of half the logic level is added to, or subtracted from, the respective counter output which is then taken to be the restored signal.

Using two counters instead of one not only decreases the number of cycles to half, but also reduces the time that must be allocated to a cycle. Each cycle must allow sufficient time to complete the required charge transfer. There are two factors that contribute to the speed of charge transfer. They are the input voltage that is necessary in overdriving the op amp, and the voltage available across the drain and source of the output transistors which supply its charging currents.

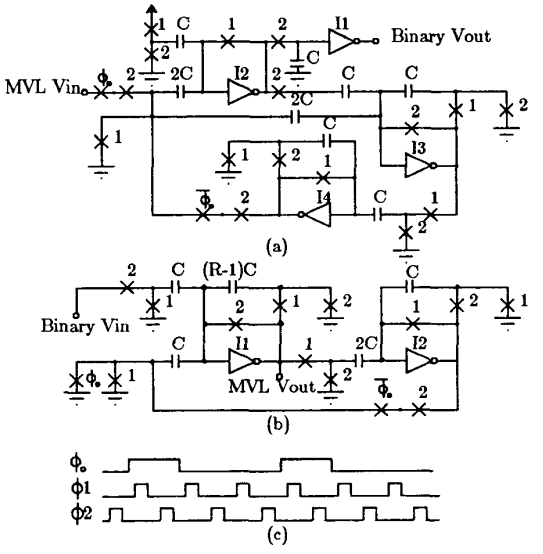

FIG 3 (a) MVL-to-Binary Converter
(b) Binary-to-MVL Converter
(c) Clock Signals

Through the use of two counters, the output will always approach the middle rather than the two ends of the power supply. Thus, a significant voltage will always be maintained across the driving transistors.

Note also that the input voltage required to overdrive the op amp is not large. For a typical gain of 60 dB, a 5mv input can drive the op amp output well beyond the middle of the 5 volt power supply. Therefore, it is possible to allow the input voltage to settle to a small value without slowing down the charge transfer significantly.

The counters use an input array of unit capacitors. The capacitors are switched on sequentially, each following the completion of charge transfer from the preceding one. If a small amount of residual charge is tolerated for each unit capacitor (clock signal frequency does not have to be so slow to allow complete charge transfer for each unit capacitor), the overdriving input voltage is maintained at all times. As a result, the op amp output will always provide the maximum possible charging current such as is available in the case of switching on all the input capacitors simultaneously. Note that, the same amount of charge can be transferred either by switching on an array of input capacitors simultaneously, as in the case of Integrator Chain (which will be discussed in section 3), or by switching on the input capacitors one by one sequentially, as it is done with this restorer. In particular, the latter will not be much slower than the former because maximum charging current is maintained at all times in both cases. This fact allows the counters to be stopped at discrete output levels, and to operate at a moderate speed which will not constitute a bottle-neck in the operation of the entire circuit.

We have observed the fact that voltage-mode MVL circuits are simple and fast, but cannot handle high base values. However, voltage-mode schemes can be combined with SC to yield a better design. Correspondingly, here a combination of a rough and a fine restorer scheme is proposed. The rough restorer is composed of one or more ratioed inverters. The fine restorer consists of a step integrator and a comparator. As shown in figure 4, one inverter used as the rough restorer

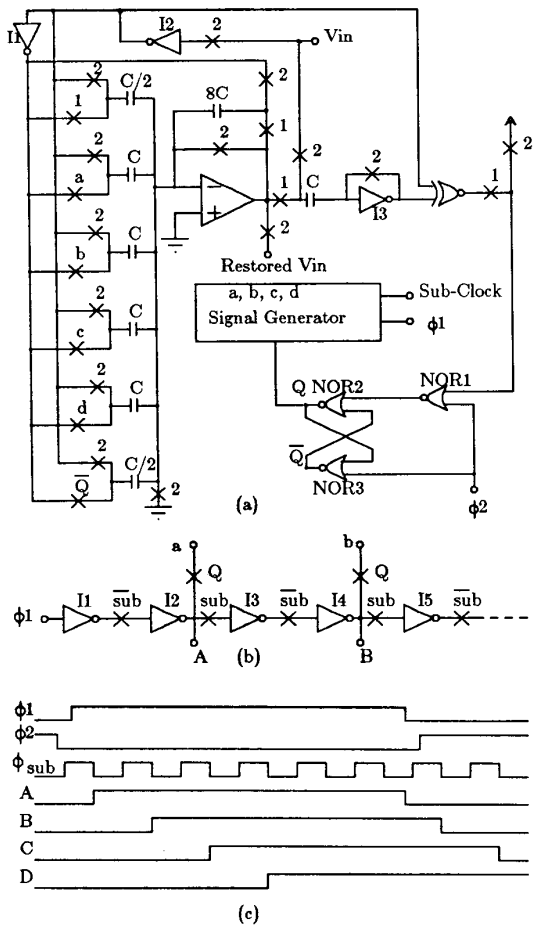

FIG 4 (a) Signal Regenerator for Radix 8
(b) a, b, c, d Generator
(c) Clock Signals

can replace one of the counters. The output of the inverter controls from which end (ground or the positive supply), the counter will start counting. The SC up-counter and down-counter each have the same structure and can be swiftly switched from one mode to the other by simply changing the sequence of switching. Using more inverters in the rough restorer will further reduce the number of counting steps required in the fine restorer.

There are a few possible methods by which to control the sequential switching of the input capacitors. A binary shift register with sub-clocking signals (as in figure 4b) is one possibility. Delay paths can also be used to obtain equally-spaced delayed versions of the main clock signal for control. However, accurate delay is difficult to create. Another approach is to monitor the completion of charge transfer for each capacitor and to switch on the next upon completion of the previous transfer. The final method suggested, shown in figure 5, uses 2 unit input capacitors switched on and off alternately by sub-clocking signals to provide stepwise input charge signals. As soon as the comparator changes state, the subclock-signal path is blocked. This method requires only one sub-clocking signal and fewer input capacitors, and is therefore preferred.

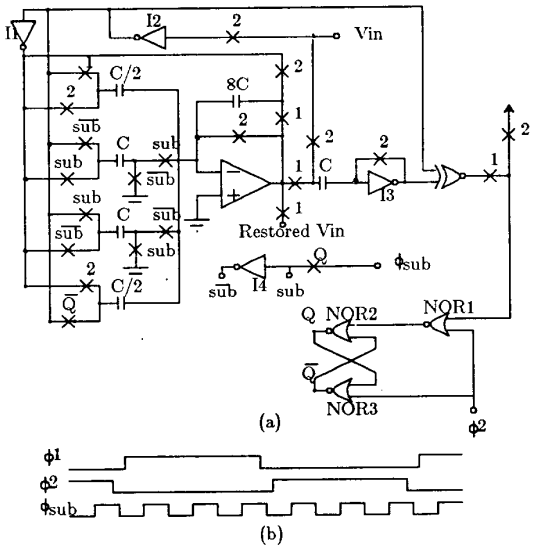

FIG 5 (a) MVL Regenerator for Radix 8
(b) Clock Signals

Basic functions, namely signal detection, provision and restoration, in MVL circuit designs have been studied and the relative merits of different modes of operation and various technologies have been briefly discussed. Now, to demonstrate the possibility of employing SC technology for MVL circuit implementation, two examples are presented. First a design of a fixed point MVL multiplier using SC technology is given. Then a general scheme for the direct realization of MVL functions by combining SC circuits and a pass- transistor structure is presented.

3. A NOVEL FIXED–POINT MVL MULTIPLIER USING SC TECHNOLOGY

A digital multiplier consists of two distinct parts, one dedicated to generation, and the other to summation of partial products. In binary, to generate partial products, NOR and NAND gates would suffice. Here signal quality would not be the concern since signal restoration is inherent in the majority of binary gates. However such is not the case for MVL multipliers. First, MVL input signals must be detected by circuits which have satisfactory speed and are not too complex or costly. As well, during partial-product generation and summation using SC technology, MVL signals will deteriorate and restoration must be performed. Cost is the main concern in this SC MVL multiplier design, since SC is intrinsically slower than other technologies and the multiplier is clearly not going to be the fastest in the world.

3.1. Partial–Product Generation

An SC integrator chain, used for the MVL coefficient multiplier design, will now be described.

Whereas most multiplication methods generate only the needed partial products, the Integrator Chain generates all possible partial-products in a sequence from which the needed ones are selected at an appropriate time.

The Integrator-Chain supplies partial products in the following sequence:

$$Y\times1, Y\times2, \ldots\ldots, Y\times k, \ldots\ldots Y\times(R-1)$$

where Y is a coefficient related to the application as shown in figure 6. Y can be provided either directly as a number of MVL reference voltages feeding unit capacitances, or indirectly using one voltage feeding an array of weighted capacitors. Since multiple MVL references can be eliminated in the latter method, it has been selected. As implied in figure 6, the partial products are strobed into capacitor memory when the respective input digits(x_j) equal k. The results remaining in the memory bank (the capacitor array) are later summed and restored to obtain the final product.

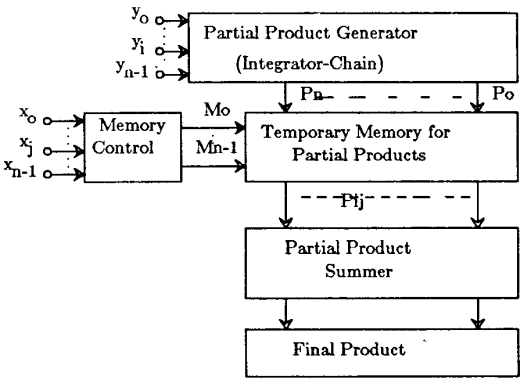

FIG 6 Block Diagram for the SC NxN Multiplier

One stage of the Integrator-Chain schematic is shown in figure 7. The op amp acts as a step integrator whose step size is controlled by the input capacitor array which represents one digit of the MVL coefficient .

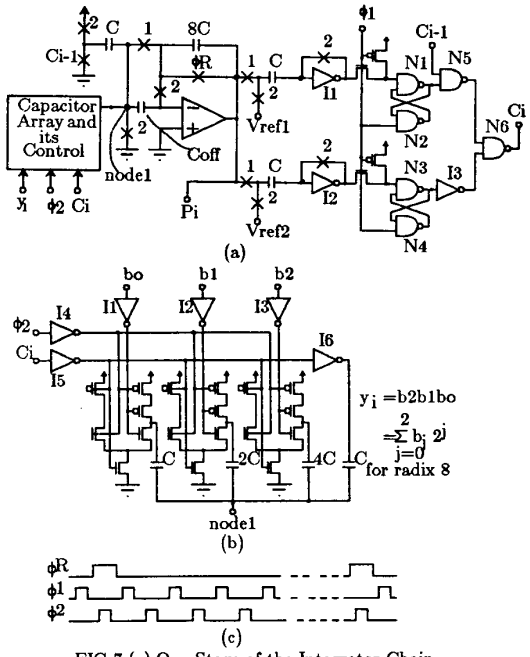

FIG 7 (a) One Stage of the Integrator-Chain
(b) Capacitor Array and its Control ,
(c) Clock signals

Error can be reduced by using C_{off} to compensate the DC offset and finite gain of the op amp. Note that the error introduced by capacitor mismatching is minimized by using the same capacitor array(figure 7b) to implement both input and charge subtraction when the carry becomes high.

A ripple scheme is used to generate carries. There are two voltage references supplied by two SC single-stage gain circuits. One provides a logic value of 6.5(V_{ref1}) and the other 7.5(V_{ref2}). The carry(C_i) will be set to high either when the output of an integrator is higher than 7.5, or higher than 6.5 and the preceding carry(C_{i-1}) is high. In this case, one unit of charge will be added to the next stage and 8 units of charge will be subtracted from the carry-creating integrator.

If step-incrementing, carry-generating and charge-adding and subtracting are done in a single clock phase, the maximum output value of the integrators can be limited to the base value. A larger logic separation and thus better noise immunity will result.

Since comparison and subtraction are done in the same phase, the integrator outputs might rise and fall in the same phase. Thus a latch(consisting of 2 NAND gates) must be added to the conventional SC comparator to maintain the comparison output constant through the clock phase.The output of the latch is set to low as Φ_1 is low and will toggle to high when the output of the SC comparator becomes low(designating the output of the integrator is higher than the reference) and Φ_1 is high. The latch output will remain high even the output of the SC comparator changes to high again. Note that positive feedback may be employed to sharpen the transition of the comparators.

Referring to figure 7b showing the capacitor array and its control, during phase 2(Φ_2), the carry C_i is always low (from figure 7a) and b_j will control which capacitor in the array is to be charged. During phase 1 (or Φ_2), the capacitor previously charged will be discharged through ground and node 2 (n_2). However, as soon as C_i becomes high, all the capacitors in the array will be charged up again, including the unit capacitor connected only to C_i. This unit capacitor serves to provide a subtraction of 8 units of charge instead of 7 otherwise.

3.2. Memory Bank

All possible partial products are generated in sequence and the products selected are written into a memory bank which is controlled by a memory-control circuit (figure 8). The con-

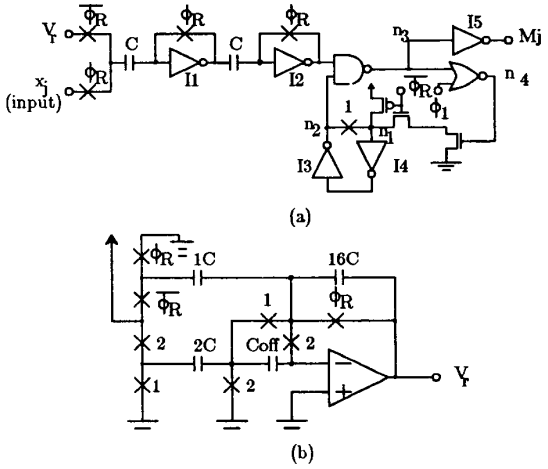

FIG 8 (a) Memory Control Comparator
(b) Voltage Reference Generator

trol circuit consists of a step reference generator (MVL counter) and a number of comparators. Each comparator must strobe in one and only one partial product between occurrences of the Reset clock signal. Here, a dynamic latch scheme is applied. Referring to figure 8a, the Reset signal($\overline{\Phi_R}$) sets node 1 (n_1) and node 2 (n_2) to high. The comparison result can pass through the NAND gate to provide the WRITE signal. However, as node 3 (n_3) goes low and node 4 (n_4) goes high, nodes 1 and 2 will go low and node 3 is forced high until the next Reset. The NOR gate is there to provide delay between n_3 and n_4 to make the WRITE signal a pulse (extending to the falling edge of Φ_1) instead of a spike. The latch will not be triggered until Φ_1 goes low even when n_3 is low because n_4 remains low. The voltage reference is generated by an MVL counter (figure 8b), where the 1C is used to create a half-logic-level immediately after Reset and the 2C is used to provide a full-logic-level increment to obtain a sequence of reference voltages of 0.5, 1.5, and so on.

The memory bank is simply a capacitor array with switches (figure 9). One memory bank is used if the system allows the partial-product-generation process to start after the previous final product is produced, and after the memory is relinquished. Otherwise, two arrays would be required and partial-product generation and summation would be performed in parallel.

3.3. Partial–Product Summation

Summing can be done using either a parallel or a serial structure.

A parallel scheme ensures that all the partial products can be summed up in one clock cycle. It can consist either of 2-input adders or of multiple-input adders. However, both types of SC adder have the same structure and each adder contains at least one op amp. Thus, overall, the scheme requires more adders and is therefore more costly. For a 4 x 4 multiplication, 15 2-input adders are required. Alternatively, a 4-input adder can be used. However such an adder yields poorer signal quality, as additional logic levels must be accommodated within the finite supply-voltage range. A 4-input design uses 7 adders for 4 x 4 multiplication along with a more complex carry- generating circuit which has to detect not one but 3 thresholds.

The serial scheme (figure 10) is much slower but less expensive. It uses 3 2-input adders or 1 4-input adder and requires 7 cycles to complete each 4 x 4 multiplication. Since one adder must sum up different digits in sequence by multiplexing, the parasitic effect of long connection lines to the memory bank will be more significant.

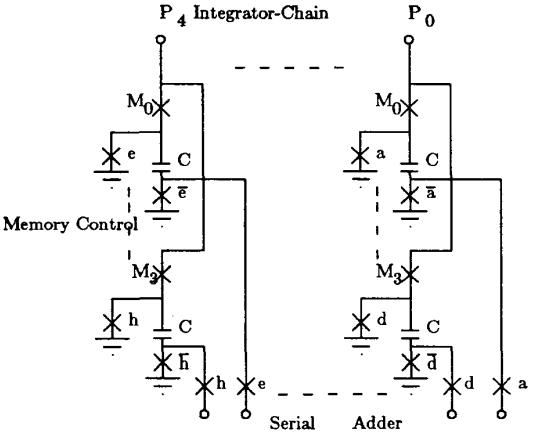

FIG 9 (a) Memory Bank for 4x4 Multiplication
(b) Clock Signals

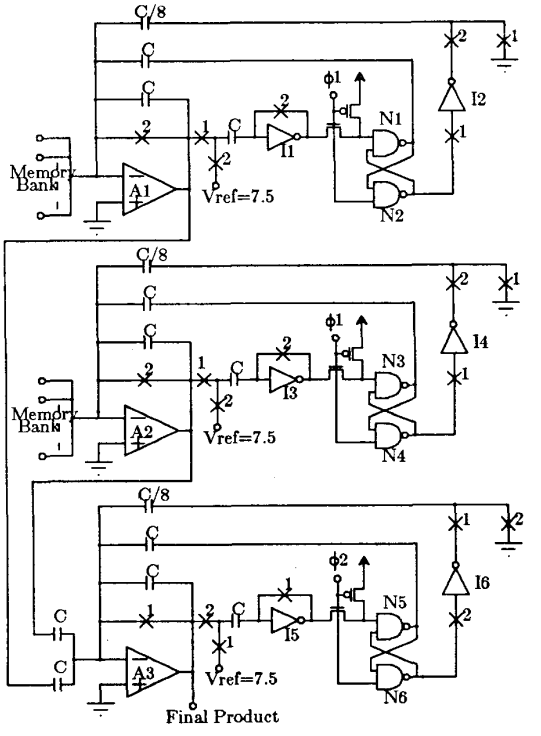

FIG 10 Serial Adder for 4x4 Multiplication

3.4. Signal Restoration

In contrast to binary logic, MVL signals having generally lower noise margins, and tend to require more frequent restoration. Having selected a satisfactory signal restorer (figure 5) from section 2, now the question is where to put it. Here the decision should be made based on performance and cost. If restoration is done in every cycle and at every point of the circuit, signal quality is guaranteed, but the cost is unrealistically high. For the SC MVL multiplier, the nodes that require signal restoration are the outputs of the Integrator Chain and the output of the final product. With restoration, the accumulated error will be eliminated from the partial product. Since a single integrator output may feed several capacitors, restoration done here is more efficient. Error can again occur during summing of the partial products, mainly as a result of large parasitic capacitances along the connection lines to the capacitors in the temporary memory. Ultimately, the final product must be restored.

3.5. Remark

The multiplier described has moderate speed and complexity. The two major characteristics of SC technology, namely base-value-independent behavior and natural occurrence of low-cost memory, are fully exploited. For base-R operation, it requires R cycles to complete partial-product generation independent of the lengths of the multiplier and multiplicand. However, the number of components increases linearly as the lengths of the multiplier and of the multiplicand increase. In the design presented, the speed of a parallel structure and the low cost of serial operation are effectively combined.

4. SC AND PASS–TRANSISTOR COMBINATIONS

The usual pass-transistor scheme is a simple and straightforward idea. It uses strings of transistors as switches, controlled by a bank of literals, to connect the desired logic signal to the output. The basic structure is shown in figure 11, where X indicates a switch (or a pass transistor).

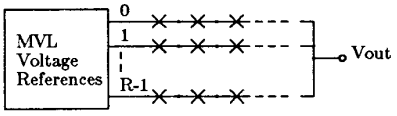

FIG 11 Basic Pass-Transistor Structure

The direct realization of an MVL function using literals, MIN and MAX, can be easily implemented with this circuit structure [7] [8] [9] [10]. The series connection of the switches represents the MIN function while the parallel connection of the strings represent an OR function. Note that this OR function is not directly the MAX function. In particular, the high logic values will not overpower the lower ones as in the case of MAX. Therefore, a slight modification of the MVL function expression is required, and conduction of different strings must be made mutually exclusive. For example, a 4-input quaternary function can be implemented as follows:

$$F(x) = f_0 + f_1 + f_2 + f_3 \qquad (4.1)$$
$$= f_0 + 1({}^0X_1^1\,{}^2X_2^2\,{}^1X_3^3\,{}^2X_4^2) + 2({}^1X_1^1\,{}^3X_2^3\,{}^2X_3^3\,{}^1X_4^2) + 3({}^0X_1^2\,{}^2X_2^3\,{}^1X_3^1\,{}^2X_4^2)$$

It can be observed that f_1 and f_3 both contain a term:

$$({}^0X_1^1\,{}^2X_2^2\,{}^1X_3^1\,{}^2X_4^2).$$

Two transistor paths will conduct simultaneously at this particular input combination if the formula is directly implemented by a pass-transistor circuit without any modification. The resulting output would be ambiguous. Since the plus sign (+)indicates a MAX function, the desired output value at this particular input should then be 3.

Therefore, the term $1({}^0X_1^1\,{}^2X_2^2\,{}^1X_3^3\,{}^2X_4^2)$ must be changed to $1({}^0X_1^1\,{}^2X_2^2\,{}^2X_3^3\,{}^2X_4^2)$ to correspond.

For more complex expressions, detection of every single overlap cannot possibly be guaranteed. One simple means to avoid this problem is to use only base literals (${}^aX^a$), though this restriction can increase the circuit complexity greatly.

Another point to note is that an MVL formula does not usually contain the term f_0 because a MIN gate is used to provide the zero logic value in default, when any literal in a product is zero. However, for the pass-transistor scheme, the zero must be supplied separately since the output does not automatically assume a logic value of zero when all the strings are at the high impedance state. In this case, the zero term would be added explicitly as follows:

$$f_0 = 0(\overline{{}^0X_1^1\,{}^2X_2^2\,{}^1X_3^3\,{}^2X_4^2}) \bullet (\overline{{}^1X_1^1\,{}^3X_2^3\,{}^2X_3^3\,{}^1X_4^2}) \bullet (\overline{{}^0X_1^2\,{}^2X_2^3\,{}^1X_3^1\,{}^2X_4^2}) \qquad (4.2)$$

A binary-to-quaternary decoder with a pass-transistor structure has been proposed by Current [11], and various MVL functions realized by pass-transistor schemes have also been proposed by Tatsuki Watanabe[8]. However, what has been neglected in most of the previous papers is the method by which the voltage references are supplied. In general, the issues of speed and signal deterioration have seldom been discussed. But the fact remains, speed and signal quality are the major measures of merit of any scheme or circuit.

Voltage signals used as logic references can be provided by MVL buses or can be locally generated. The latter approach is preferred, for it may occupy less space in a VLSI implementation. Voltage references can be locally generated by a voltage divider, perhaps a stack of diode-connected MOS transistors as suggested by Current in his binary-to-quaternary decoder circuit[11]. However, the disadvantage of this method is the large constant biasing current required by the large MOS devices needed to ensure sufficient driving capability. Another drawback is that the limited number of voltage signals that can be generated by a MOS stack restricts its use for high-radix operation.

In contrast to MOS stacks, SC circuits provide virtually no limit in generating any desired voltage value. As well, the low output impedance of the op amps used in SC ensures a much greater driving capacity than does a MOS stack.

The limitations of operational speed and signal deterioration of a pass-transistor circuit are largely due to the series impedances and stray capacitances of the transistor paths. In the worst case, a voltage reference must charge or discharge not one but all the paths connected to the same output node. If the radix used is high, and more paths are required, the total charge to be supplied can be very large. As well, signal restoration may be needed at some points in a circuit, and a signal restorer in any MVL technology is typically non-trivial.

Because, at any moment, only one logic value is connected to an output, one op amp would suffice. But now the pass- transistors are not in the signal path, but rather become part of the control circuit. The nodes that were once used to connect to various voltage references are now used to control the SC adder, and the node that was the output is now connected to the power supply. A quaternary schematic illustrating this idea is shown in figure 12.

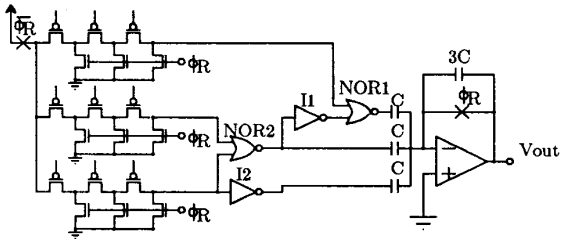

FIG 12 Quaternary SC-Pass-Transistor Circuit *

It is obvious that this design does not require the explicit term f_0, because every time the output of the op amp is reset to zero, it remains at zero if no charge transfer is provoked. Through the OR gates, the paths of lower logic value are masked by the higher logic-value paths to effect the MAX func-

* In FIG 12 and FIG 13, the PMOS transistors are Controlled by literals

tion. Overlapping of product terms as in a normal MVL formula is therefore allowed. This relaxation can lead to fewer logic gates and a simpler structure for the literal gates to be used. For instance, an MVL function

$$f(x) = 1({}^0X_1^1\ {}^0X_2^2\ {}^3X_3^3) + 2({}^0X_1^2\ {}^3X_2^3\ {}^3X_3^3) + f_0 \qquad (4.3)$$

can be converted to

$$f(x) = 1({}^0X_1^1\ {}^3X_3^3) + 2({}^0X_1^2\ {}^3X_2^3\ {}^3X_3^3). \qquad (4.4)$$

A slightly modified version of this circuit is shown in figure 13. While this scheme is slower in discharging the nodes to ground because of the series connection, there is no effect on overall speed if a 50%-duty-cycle clock is used and the speeds of charging and discharging are the same. This particular structure is well-suited for the diffusion-line- layout method and some area reduction can be expected.

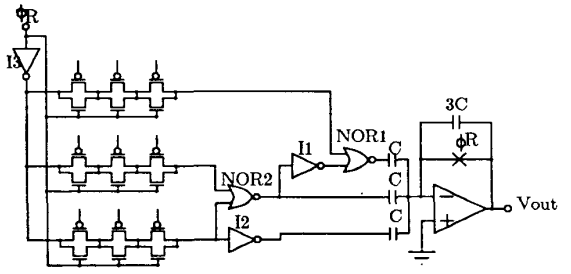

FIG 13 Modified Version of FIG 12 *

Regarding the speed of operation for the normal pass-transistor scheme, the output node has to be charged to the intended logic reference value through the switch string, and the transfer of the last few percent of charge is always the most time-consuming. In the case of the SC version, the voltages at the ends of the paths need only reach the thresholds of the inverters. As these thresholds are usually in the vicinity of the middle of the power supply range, the time required is expected to be quite short.

The deviation from ideal of the logic signals obtained from the output of the SC adder is caused by 1%-of-maximum capacitor mismatch, dc offset and finite gain of the op amps, and parasitic capacitances. This error can be reduced greatly by compensation techniques well-developed in conventional SC technology.

5. CONCLUSIONS

In this paper, three basic functions, namely signal detection, provision and restoration, required of all MVL circuits, have been discussed for each of the 3 signal modes in various technologies. Alternative schemes using switched-capacitor (SC) techniques have been introduced. In particular, an SC MVL multiplier design has been proposed. The SC multiplier design is topologically base-independent. The size (and device counts) of the complete circuit may be drastically decreased in comparison to other schemes if a higher base value can be used. This may be particularly attractive in the future as greater control of fabrication technology is achieved. As well, a special combination of pass-transistor structures and SC circuits, having some useful performance improvement, has also been presented.

In this work, it has been demonstrated that MVL signals can be easily generated and manipulated in an SC system. The natural occurrence of low-cost memory in SC circuits has been exploited to obtain the speed advantage of parallel structures while maintaining low device counts. The simplicity of voltage-to-time and time-to-voltage conversion makes the trade-off between speed and space a trivial task. Circuit complexity can be greatly reduced in cases where low-speed applications allow extra speed to be sacrificed. It is also observed that for these circuits the natural base e is far from optimal. In fact, for SC circuits, the base value should be very much higher to effect more efficient use of op amps, which are the major components in an SC circuit and not inexpensive.

For the same reasons, the approach which uses the SC literal, SC MAX and SC MIN gates for direct realization of MVL functions, is not recommended. In fact, the SC technique is suited primarily to gates having greater (system) functionality. However, in combination with pass-transistor structures, SC circuits can be applied to implement MVL functions expressed in terms of literals, with MAX and MIN, in ways which bring some improvement over conventional pass-transistor schemes.

In conclusion, for MVL implementation, SC technology can be as good as other technologies, and may even be better in some applications.

6. ACKNOWLEDGEMENTS

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